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STUDY OF CONTEMPORARY ELECTRONIC COMPONENTS UNDER
A FLUID-PRESSURE ENVIRONMENT

RESEARCH TRIANGLE INSTITUTE

PREPARED FOR
NAVAL SHIP RESEARCH AND DEVELOPMENT LABORATORY

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STUDY OF
CONTEMPORARY ELECTRONIC COMPONENTS
UNDER A FLUID-PRESSURE ENVIRONMENT

by

J. W. Harrison

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PREFACE

This report was prepared by the Research Triangle Institute, Research Triangle Park, North Carolina, for the Navy Ship Research and Development Center (NSRDC), Annapolis, Maryland, under contract no. N00690-72-C-0506. The study was conducted in the Engineering Division by Drs. J. J. Wortman and J. W. Harrison. The study was conducted during the period November 1971 through March 1973.

This work was administered under the direction of Mr. Martin J. Siegwann of NSRDC.

Publication of this report does not constitute Navy approval of the report's findings or conclusions. It is published only for the exchange and stimulation of ideas.

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ABSTRACT

The effects of a high fluid pressure environment on electronic components has been examined with emphasis on semiconductor devices including integrated circuits. The impetus for this study has been the possible application of electronic systems in the deep ocean without protection from the large hydrostatic pressure of that environment.

The effects of both the fluid and the pressure on components immersed in oil at pressures up to 15,000 psi have been considered theoretically, with experimental verification when possible. It is concluded that structurally homogeneous electronic materials such as silicon and germanium will not be affected by the high pressures. Similarly, while the fluid and the impurities contained in it can potentially cause changes in semiconductor device properties, none are expected to occur because of the advanced manufacturing and packaging techniques currently employed for such devices. The effects of pressure will be most evident on components containing voids within the package. For example, metal enclosures for semiconductor devices will be deformed at pressures equivalent to immersion at several hundred foot depths in the ocean.

Pressure hardening techniques involving free flooding and component structure design are described.

STUDY OF CONTEMPORARY ELECTRONIC COMPONENTS UNDER A FLUID-PRESSURE ENVIRONMENT

1.00 INTRODUCTION

The purpose of this report is to document the results of a study to determine the influence of a fluid-pressure environment on contemporary electronic components. The study has been concerned with: (1) an identification of problem areas, (2) evaluation of devices and components in view of problems, (3) identification of failure modes and techniques to prevent failures, and (4) development of technology to be used to harden as many components as possible for use in undersea applications. The results reported here are based on both theoretical and experimental considerations. Due to the complexity and size of the total problem of outboard electronics, the study has of necessity been limited to critical areas with many interesting and needed considerations forgone in the interest of time and funds.

1.1 Past Work and Future Needs

The desire and indeed the successful accomplishment of outboard electronics is not new. As early as 1959 [Ref. 1], testing was started to determine the effect of deep ocean pressures on both passive components, resistors, capacitors, inductors-transformers, and thermistors and active components, transistors and batteries. Subsequent tests were performed in the same manner [Refs. 2, 3, 4]. The approach was strictly empirical. Typically used components were selected and circuit parameters, resistance, capacitance, inductance, leakage, currents, etc. were monitored to determine their change in value versus pressure. Insofar as components could be generally classified by type, the results were similar:

1. Carbon-composition resistors usually changed value by $-20\%/1000$ atmospheres to $-30\%/1000$ atmospheres. Wire wound or film type resistors usually exhibited little change in resistance with pressure.
2. Capacitors of completely filled construction, such as molded or dipped mica, glass, mylar and impregnated paper types, usually showed small change in capacitance with pressure. Exceptions were traceable to internal voids. The effects of these voids were more noticeable for tantalum and aluminum electrolytic capacitors, which usually exhibited severe case deformation and often failed.
3. Inductors and transformers with laminated cores usually exhibited little parameter value change (inductance or voltage ratio). However, porous core structures such as permalloy dust, tape wound and ferrites were found to exhibit large value changes with pressure.
4. Transistor cases crushed at pressures which depended upon size, the larger the case size usually the lower the pressure at which it failed.

A few attempts at modification were made. Potting was found to be effective in increasing component pressure resistance, particularly when a flexible silicone rubber under coat was used prior to the addition of a more rigid outer cover such as epoxy [Ref. 2]. Potting of complete circuits was also found to be effective [Ref. 2]. Another technique, flooding, was also found successful, at least on a short term basis. Flooding with oil was used on transistors [Refs. 2, 3] without evidence

of contamination up to a month. Flooding a permalloy dust core with oil reduced the maximum change in inductance with pressure from 32 percent to one percent [Ref. 2].

This previous work has been empirical, generally an attempt to find usable components to fulfill a particular need. In some cases, the designation and manufacturer of the components tested has been given [Refs. 1, 4]. In other cases, due to the required brevity of the article, such information is sketchy [Ref. 2] or completely absent [Ref. 3]. The reported results lead to the general maxim: avoid voids. Other general conclusions are difficult to draw, however.

More recently there have been two activities within the Navy in this field. The first of these has been at the Navy Ship Research and Development Center at Annapolis, Maryland [Ref. 5]. This work has been concerned primarily with a review of the total problem of outboard electronic systems and consequently considering such important problems as selection of the pressurizing fluid. Reference 5 contains many important references and summaries of past work. The other Navy study is being performed at the Naval Undersea Center, Hawaii Laboratory [Ref. 6]. This work has concentrated on evaluating the feasibility of utilizing off-the-shelf electronic components. Numerous devices have been identified as potential candidates for outboard applications.

The present study is in direct support of the NSRDC effort. Emphasis has been placed on obtaining fundamental information for use in characterizing the influence of a fluid-pressure environment on electronic components and to identify pressure hardening techniques to qualify devices which will not withstand the environment. Because a fair amount of work has been reported to date on passive components, the emphasis of

the present program has been to formulate an analysis that will explain the previous test results. For semiconductor components, however, a more ambitious program has been undertaken. This has been done for two reasons: first, the amount of past work reported in this area is slight, and in little detail; second, the recent trend in integration of devices and components in semiconductor microcircuit form has and will continue to revolutionize circuit design. If a study of pressure effects is to be of value to designers of future Navy outboarded equipments, it must deal with those devices and components that designers must use to carry out the increasingly complex operational and explorational missions of this decade and beyond.

A discussion of the semiconductor devices most likely to be used and the justification for selection of representative types is given in Section 1.2 below. Chapter 2.0 presents an analysis of the effects of pressure on component housings and packages, including a discussion of methods of reinforcement or redesign to improve pressure resistance. Chapter 3.0 deals with the problems caused by direct exposure of component internals to the pressurizing fluid. Chapter 4.0 presents a summary of the results of the study to date and their relation to the anticipated problems. Chapter 5.0 gives our recommendations for further research.

1.2 Selection of Devices for Testing

In order to obtain an idea of what components are most likely to be used in systems designed in the near future for outboarding, which components must necessarily be tested for pressure tolerance, we first look at several system types that would possibly be outboarded. For convenience, we divide these into categories of electronic power supplies, sensing and signal processing systems, information processing and control systems, and power and propulsion control systems. Tables 1.1, 1.2, 1.3

Table 1.1: Major Components in Electronics Power Supplies

A. Discrete Components

1. Transformers
2. Inductors
3. Capacitor
4. Rectifiers
5. Series Pass Regulator
(Power Transistor)
6. Resistors (Divider and
Bleeder networks)
7. Thyristors (SCR, TRIAC, etc.)

B. Integrated Circuit Components

1. Voltage and current sensing and
control
2. Reference voltage supplies
3. Zero-voltage switching control

C. Fabrication Components

1. Hard wire and solder
2. Heat sinks
3. Circuit board (hard wire or p.c.)
4. Device sockets and board connectors
(plug in)
5. Metal chassis, brackets, etc.

Table 1.2: Major Components in Sensing and Signal Processing Systems

- A. Discrete Devices
 - 1. Crystals (reference oscillators, filters)
 - 2. Delay lines
 - 3. Transistors
 - 4. Diodes
 - 5. Capacitors
 - 6. Resistors
 - 7. Inductors
 - 8. Transducer elements
- B. Integrated Circuit Components
 - 1. Linear IC's (op amps, references)
 - 2. Non-linear IC's (comparators, one shots, D/A and A/D converters, function generators, etc.)
 - 3. Digital IC's
- C. Hybrid Components
 - 1. Linear chips
 - 2. Non-linear chips
 - 3. Digital chips
 - 4. Passive component chips or pellets
- D. Fabrication Components
 - 1. Hard wire and solder
 - 2. Heat sinks
 - 3. Circuit board (hard wire or p.c.)
 - 4. Hybrid substrate and lead frame
 - 5. Device sockets and board connectors (plug in)
 - 6. Coaxial cable or shielded multi-pair
 - 7. Chassis, brackets

Table 1.3: Major Components in Information Processing and Control Systems

- A. Integrated Circuit Components
 - 1. Gates for in/out routing, control
 - 2. Shift registers
 - 3. Arithmetic processors
 - 4. Flip-flops
 - 5. Programmable memory
 - 6. Read only memory
- B. Discrete components
 - 1. Crystals (reference oscillators - clock)
 - 2. Delay lines
 - 3. Transistors
 - 4. Passive components
- C. Hybrid Components
 - 1. Transistor and diode chips or pellets
 - 2. Passive component chips or pellets
- D. Fabrication Components
 - 1. Hard wire and solder
 - 2. Heat Sinks
 - 3. Circuit board (hard wire or p.c.)
 - 4. Hybrid substrate and lead frame
 - 5. Device sockets and board connectors (plug in)
 - 6. Coaxial cable or shielded multi-pair
 - 7. Chassis, brackets

and 1.4 give, respectively, a listing of the components commonly found in systems of these types. These components are divided into discrete components, in other words, those components containing only one device; integrated circuit components in which a variety of electronic functions are performed in one package; and fabrication components including the hardware that is necessary to interconnect and mount the discrete and integrated circuit components. Another category which is included is that of hybrid components. The hybrid components are those components which serve a multifunction purpose and are different from integrated components in that they may be composed of several chips and may be used in the same circuit with discrete device components, all mounted in one package.

These listings are not meant to be exhaustive, but are meant to give an indication of the variety of components which must be investigated and must be proved to be pressure tolerant or proved to be modifiable to pressure tolerance in order that the systems of these types may be constructed for outboarding in submersible vehicles. With these listings as a guide, we now go on to discuss the justification for including the semiconductor device components which are considered to be useful to the systems designer, both in the immediate future and several years from now.

Discrete transistors for a long time to come are most likely to be used in power applications, that is, in those applications which require the handling of high currents or high voltages in a circuit. Except for relatively rare occurrences, such as mentioned in [Ref. 7], placement of power transistor structures on an integrated circuit chip is impractical due to the large area required and because of the heat generated during operation. Large areas increase the probability of manufacturing defects

Table 1.4: Major Components in Power and Propulsion Control Systems

- A. Integrated Circuits
 - 1. Linear IC's (op amps, references)
 - 2. Non-linear IC's (D/A converters, one shots)
 - 3. Digital IC's (flip-flops and logic functions for alarms, interlocks and switching control)
- B. Discrete Components
 - 1. Rectifiers
 - 2. SCR's (uni- and bi-directional)
 - 3. Power transistors
 - 4. Capacitors (commutation, coupling, filtering)
 - 5. Resistors
 - 6. UJT and four-layer devices
 - 7. Transformers (pulse and power)
 - 8. Inductors
 - 9. Electromechanical contactors
 - 10. Surge and RFI suppressors
- C. Fabrication Components
 - 1. Hard wire and solder
 - 2. Heat sinks
 - 3. Circuit board (hard wire and p.c.)
 - 4. Hybrid substrate and lead frame
 - 5. Device sockets and board connectors
 - 6. Coax cable or shielded multi-pair
 - 7. Chassis, brackets, etc.

due to the presence of crystallographic faults in the silicon wafer, or due to inhomogeneous conditions over the wafer's surface during one or more of the processing steps in constructing the circuit. In addition, the large power dissipation of a power transistor structure means that the heat must be dissipated and that the surrounding area of the chip is raised to a fairly high operating temperature. If this can be possibly avoided in the small signal circuits, it is desirable to do so. For these reasons, it seems most likely that far into the future, whenever small signal processing components and power transistor components must be used in the same circuit, that the power transistor components will be separately mounted away from the small signal processing circuit chips so that the power dissipation of the higher power components can be adequately taken care of without undue temperature rises in the small signal circuits.

The next category of components is that of small scale, or medium scale, integrated circuits. These are used in relatively simple systems, such as those for sensing and signal processing, or those for exercising control. Table 1.5 lists a few applications of some small scale, integrated circuits in typical systems for signal processing such as communications.

A wide variety of operational amplifiers and small scale integrated circuits are available for linear signal processing, such as amplification, and filtering of signals. These small signal integrated circuits operational amplifiers may also be used for nonlinear applications, such as modulation, demodulation and waveform generation and shaping. However, some specialized units are also constructed for modulator/demodulator units for constant voltage regulation and for constant current regulation. In addition to these linear devices and specialized nonlinear devices, also there are

Table 1.5: Typical Applications of Small Scale Integrated
Circuits in Signal Processing

Amplification (DC, Audio, Video)
Balance to un-balance level shift
Automatic tuning and gain control
Active network filtering (continuous)
Analog operations (integration, summing, etc.)
Impedance matching
Timer and synchronization functions
Digital filtering
Signal modulation and demodulation

linear/nonlinear combinations which are used in circuits such as sample and hold circuits A/D and D/A converters, multiplier/dividers and similar circuit types.

Digital IC devices also can be obtained in small scale IC form, but may also range up to very large scale IC form. Examples of the small scale digital IC's are hex inverters and flip-flops, and examples of large scale devices are shift registers, programmable random access memories (RAM's) and read-only memories (ROM's). A comparison of the major IC digital logic families taken from a recent survey [Ref. 8] is available for various circuit design implementations, is shown in Table 1.6. Another table, Table 1.7, shows the availability of various functional types and the respective families [Ref. 8]. Since the referenced article was published in December 1970, many additional functional types have become available, particularly in MOS and CMOS circuit implementations.

In addition to the bipolar transistor type logic families, such as the TTL, DTL, and ECL families, the MOS and CMOS structures are rapidly becoming major building blocks in circuit design. This is because important improvements have been made in reducing the area committed to the building block device in these digital IC circuits and due to the fact that many of the MOS type circuits can be made much more reliably than they were when they were initially introduced onto the market. The advent of "self-registering" MOSFET structures has enabled greater fabrication simplicity, higher functional packing densities and ease of circuit design for high speed operation [Ref. 9].

Table 1.6: Availability of functions for various IC families [Ref. 8]

	RTL	DTL	HTL	TTL	ECL	PMOS	CMOS		RTL	DTL	HTL	TTL	ECL	PMOS	CMOS
Gates:								Arithmetic functions:							
AND	X	X	X	X	X			Adder	X			X	X	X	X
NAND	X	X	X	X	X	X	X	Look ahead carry block				X	X		
OR	X	X	X	X	X			5-bit adder	X			X	X		
NOR	X	X	X	X	X		X	Max. value comparator				X	X		
Exclusive OR	X	X	X	X	X		X	Arithmetic unit				X	X		
Exclusive NOR	X	X	X	X	X		X	Round-through multiplier				X	X		
OR/NOR	X														
A-O-I	X	X	X	X				Shift registers							
Inverters	X	X	X	X	X		X	2-bc		X	X	X	X		
Expanders	X	X	X	X	X			4-bc	X			X	X		
AND/OR select							X	8-bc				X	X		
								Multibit (serial)					X	X	
Flip-flops:								Memories:							
R-S	X	X	X	X	X		X	8-bit RAM				X	X		
Latch	X	X	X	X	X			16-bit RAM				X	X	X	X
"T"	X			X	X			64-bit RAM				X	X	X	X
"D"	X	X	X	X	X		X	256-bit RAM				X	X	X	X
J-K	X	X	X	X	X			256-bit ROM				X	X		
Counters								4096-bit ROM				X	X		
Divide-by 20	X	X	X	X	X		X	Large serial access				X	X		
Divide-by 12				X	X			read/write				X	X		
Divide-by 16	X	X	X	X	X		X	CAV or CDRAM				X	X		
Programmable				X	X										
Up/down				X	X		X	Miscellaneous:							
3 stage							X	Multiplexers or data							
16 stage							X	selector	X			X	X	X	X
Decoders:								Demultiplexers or data							
BOD to decimal	X		X	X				transmitters				X	X	X	
Excess 3 to decimal				X				Line drivers (differential)	X	X		X	X		
BOD to 7 segment				X		X		Line receivers (differential)	X	X		X	X		
4 to 16 lines				X				Translators	X			X	X		
3 to 8 lines				X				Multiplexers	X	X	X				
2 to 4 lines				X				One-shots	X	X	X				
Encoders:								Pulse stretcher							
Binary to BOD				X				(retriggerable one-shot)		X	X				
BOD to binary				X				Schmitt trigger	X			X	X		
Priority				X				A/D converter				X	X		
Drivers and buffers:								Frequency/phase detector				X	X		
Line drivers		X	X	X	X			VCM (voltage controlled				X	X		
Logic drivers	X	X	X	X	X			oscillator)				X	X		
Clock drivers	X	X	X	X	X			Parity tree				X	X		
Relay drivers			X					8-bit position sense				X	X		
High fanout buffer	X	X	X	X	X		X	Sense amplifier	X			X	X		
								Prescaler				X	X		
								Comparator				X	X		

Table 1.7: Comparison chart of the major IC digital logic families [Ref. 8]

Parameter	RTL	Low Power RTL	DTL	HTL	1T1T TTL	2T1T TTL	4T1T ECL	2T1T ECL	PMOS	CMOS
1. Circuit form	—3— is inverter function—1—	—3— is inverter function—1—	—3— is inverter function—1—	—3— is inverter function—1—	—3— is inverter function—1—	—3— is inverter function—1—	—3— is inverter function—1—	—3— is inverter function—1—	—3— is inverter function—1—	—3— is inverter function—1—
2. Power logic function of basic gate	NOR	NOR	NAND	NAND	NAND	NAND	NAND	NAND	NAND	NAND
3. Worst possible logic function	Implied AND (same function)	Implied AND (same function)	Implied AND (same function)	Implied AND (same function)	Implied AND (same function)	Implied AND (same function)	Implied AND (same function)	Implied AND (same function)	Implied AND (same function)	Implied AND (same function)
4. $T_{propagation}$ delay, t_{pd}	40	1.5	15	15	10	10	15	6	2.5	1.5
5. Typical low-level V_{OL}	R_{in}	R_{in}	R_{in}	R_{in}	R_{in}	R_{in}	R_{in}	6 ohms or 2.2 mA	25k	25k
6. Fanout	5	4	10	10	10	10	25	10 loads or 10 ohms	20	50 or higher
7. Specimen temperature range, °C	—55 to 125	—55 to 125	—55 to 125	—55 to 125	—55 to 125	—55 to 125	—55 to 125	—55 to 125	—55 to 125	—55 to 125
8. V_{CC} voltage	2.0V ± 10%	2.0V ± 10%	2.0V ± 10%	2.0V ± 10%	2.0V ± 10%	2.0V ± 10%	2.0V ± 10%	2.0V ± 10%	2.0V ± 10%	2.0V ± 10%
9. $T_{propagation}$ delay per gate	12 mV	2.5 mV	8 mV or 2.5 mV	55 mV	12 mV	12 mV	40 mV	55 mV plus load	0.3 to 10 mV	0.1 mV at 10 mV
10. Immunity to external noise	nominal	low	good	nominal	very good	very good	good	good	nominal	very good
11. Noise generation	medium	low-medium	medium	medium	medium-high	high	low	low-medium	medium	low-medium
12. Propagation delay per chip	12	27	20	50	32	6	4	2	3	70
13. Typical delay into fan-out, ns	8	2.5	11 to 20	4	11 to 20	31 to 60	60 to 120	200	400	5
14. Number of functions that can be done	high	high	high	high	high	high	high	high	high	high
15. Cost per function	low	low	low	medium	low	medium	low	medium	medium to high	medium to high

The small scale integrated circuits and medium scale integrated circuits are used in those applications where the designer wishes a high functional packing density. For instance, with a small scale integrated circuit, one can obtain several transistors on one chip which takes up just a fraction of the volume of the same transistors packaged as discrete devices. The medium scale integration of operational amplifiers offers the circuit designer the possibility of almost ideal black-box type circuit design in which he can use the inherently high gain of the operational amplifier in connection with suitable feedback elements to achieve whatever gain characteristic is required in this circuit application. In addition, prepackaged medium scale integrated circuit devices, such as modulators, demodulators, multiplier/dividers or logarithmic amplifiers, can shrink the required space in a circuit and provide the circuit designer with a much reduced design problem in that he does not have to design all of the internals which go into making up such circuits, but has only to deal with the input and output terminal characteristics. For these reasons it is expected that the use of small scale integrated circuits and medium scale integrated circuits in circuit design will be very widespread and indeed, has already become common in circuit design. Since the circuit designer will be using devices of these types, it is imperative that a realistic testing program test whether or not devices of the various types of small scale and medium scale integrated circuits can withstand the pressure requirements for their application.

The saving grace in the face of the multiplicity of circuit functions is that all of these devices are based on a single technology, silicon planar technology. Therefore, only representative samples of such devices need be tested thoroughly and the behavior of these circuit functions under

the applied pressure can be extrapolated to interpret or predict what will happen with the other types of devices.

The medium scale and small scale integrated circuits used in digital logic circuits are used for a variety of functions, not only to perform logic necessary to compute or perform various mathematical functions in the digital logic circuits, but also in the design of go/no-go decision making circuits which are useful in alarm and interlock. The large scale integrated IC's will find vast application in information processing computers, in memory and control manipulations within these computers.

In computers which are designed for use at atmospheric pressure, be it land or sea, the magnetic core has found an almost preemptive place in the design of large volume storage memories for computers. However, it turns out [Ref. 7] that the ferrite core is extremely sensitive to stress and a great deal of trouble has been experienced in the past whenever these cores were potted in such a manner as to build in such strains. If the potting material applies excessive stress to the core, then unwanted effects are found [Ref. 10]. If this happens with the stresses developed in potting, it will assuredly happen also with the stresses due to hydrostatic pressure in an outboarded electronic system. Therefore, it is highly unlikely that ferrite memory cores will be used to construct the memories of outboarded computers in a pressure tolerant electronic system. In contrast, planar silicon IC's for memory are expected to be insensitive to deep ocean pressures.

In addition to the competitive feature of integrated circuit memory components and system design, vis-à-vis ferrite cores, the imagination of IC designers is providing a great many different functions for the use of system designers in implementing their ideas. The multiplicity of available functions enables a more unique design on the part of an individual

designer, and will come to advantage when the unique characteristics required of Navy systems forces the designer to cope with the required design constraints. In addition to the multiplicity of functional types available, an effort is being made by many device manufacturers now to provide compatibility among logic types. Notable in this direction is the effort of some manufacturers to make MOS type logic circuits compatible with bipolar TTL logic circuits so that a designer can intermix the two types of circuits in his system design with a minimum amount of interface difficulty. For these reasons, it seems that in the future an increasing use will be made of the many large scale integrated circuit functions and medium scale integrated circuit functions for logic circuit design of various system types.

The large scale integrated circuits will be made and are made on silicon chips, of planar geometry. However, it is not entirely safe to extrapolate the results from testing of small scale or medium scale integrated circuits to the testing of large scale integrated circuits because the chip area of the large scale integrated circuit is usually much larger. This larger area will undoubtedly result in more voids in the bond between the semiconductor chip and the header upon which the chip is mounted. Care must be taken in the examination of these devices, the LSI devices, to assure that consistently the bonding technique used to bond the chip to the substrate is such that the voids formed are much less than those likely to lead to extreme deformation or cracking of the chip under a high applied pressure.

The above discussion leads to the following rationale about testing devices which are representative of those most likely to be used in PTE applications. Because of the marked similarity of silicon planar device

processing used for practically all types of devices now available, it is necessary only to test representative devices, not test all devices.

Representative devices were selected for testing on the following bases.

1. Small signal transistors, both bipolar (npn or pnp) and unipolar (field effect) types would be expected to be sensitive to ionic contamination of their surfaces unless adequate design in fabrication has forestalled such effects through the use of passivation, field plates, "channel stoppers" or similar techniques.

2. Silicon power transistors would be expected to be susceptible to mechanical damage because of the relatively large chip area which provides a greater possibility of voids in the chip to substrate bond. In addition, some experience with heat transfer characteristics of power devices in pressurized oil was needed.

3. Germanium devices lack the oxide passivation used on silicon devices. These would be expected to be immediately affected by any ionic contamination in a pressurizing dielectric fluid.

4. Medium scale integrated circuits have relatively large chips, typically 50 to 60 mils per side. There would be a greater possibility than for smaller chips to encounter voids in the chip to substrate bond. Linear integrated circuits such as operational amplifiers would include a variety of component types on one chip such as resistors, capacitors, diodes and transistors. In addition, the input transistors operate at low signal levels and would be expected to show up any contamination effects which would be amplified through to the output stages.

The devices tested and types of test are presented in Table 1.9.

Table 1.8: Types of Devices Tested and Types of Tests

Device Designation	Function	Material	Type	Testing Type and Condition
2N4232	Power	Silicon	NPN-Plane	Pressure and contamination - Decapped TO can
2N3740	Power	Silicon	PNP-Plane	Pressure and contamination - Decapped TO can
2N1412	Power	Germanium	PNP-Alloy	Pressure and contamination - Decapped TO can
2N1553	Power	Germanium	PNP-Alloy	Pressure and contamination - Decapped TO can
2N2222A	Small signal	Silicon	NPN-Plane	Pressure and contamination - Decapped TO can
2N2907A	Small signal	Silicon	PNP-Plane	Pressure and contamination - Decapped TO can
2N526	Small signal	Germanium	PNP-Alloy	Pressure and contamination - Decapped TO can
2N3796	Small signal	Silicon	MOSFET N Channel	Contamination - Decapped TO can
3N157	Small signal	Silicon	MOSFET P Channel	Pressure and contamination - Decapped TO can
3N152	Small signal	Silicon	MOSFET N Channel	Pressure - Decapped TO can
3N140	Small signal	Silicon	MOSFET N Channel	Pressure - Decapped TO can
M164	Small signal	Silicon	MOSFET P Channel	Pressure - Decapped TO can
2N5459	Small signal	Silicon	JFET N Channel	Pressure - Plastic package
2N5462	Small signal	Silicon	JFET P Channel	Pressure - Plastic package
2N2484	Small signal	Silicon	NPN-Plane	Pressure and contamination - Decapped TO can
2N2483	Small Signal	Silicon	NPN-Plane	Contamination - Decapped TO can
2N706	Small signal	Silicon	NPN-Plane	Contamination - Decapped TO can
2N2995	Small signal	Silicon	PNP-Plane	Pressure - Decapped TO can
2N3962	Small signal	Silicon	PNP-Plane	Pressure - Decapped TO can
SN7473N	Dual J-K Flip/Flop	Silicon	Plane	Pressure - Plastic package

Table 1.8: Types of Devices Tested and Types of Tests (cont'd)

Device Designation	Function	Material	Type	Testing Type and Condition
7000	Frequency Compensated Operational Amplifier	Silicon	Plane - 20 transistors, 12 resistors, 1 capacitor	Pressure - Detached TO can
7007	Precision Operational Amplifier	Silicon	Plane - 20 transistors, 4 diode-connected transistors, 11 resistors	Pressure - Detached TO can Pressure - Ceramic packages

2.0 EFFECTS OF PRESSURE ON COMPONENT HOUSINGS AND PACKAGES

2.1 Introduction

Component housings typically present a large surface area over void regions. Generally, the thickness of the material is sufficient to protect against random blows in an atmospheric ambient, but not sufficient to resist deformation under large hydrostatic pressures. Such deformation may result in damage due to shorting of electrical circuits, catastrophic collapse or stress amplification that leads to failure of the component internal to the package. These possibilities make it imperative to analyze the deformations that will occur in typical component package configurations and to determine the maximum allowable hydrostatic pressure for a given package type.

The well known methods of linear elastic theory are used in this chapter for the analysis of the mechanical stress distributions which result in component packages when subjected to hydrostatic pressures. The usual assumptions [Refs. 11, 12] made in such an analysis are employed here, namely that

1. the materials are perfectly elastic;
2. the materials are homogeneous and isotropic; and
3. superposition of stresses (or strains) is permissible.

These assumptions allow the use of relatively well developed models to determine at what hydrostatic pressures the limiting value of elastic stress is reached. This is the yield point stress. Beyond this stress, permanent deformations occur and the assumptions listed above are no longer valid.

In many, if not most, cases the yield point may be reached at some point in one or more regions of a component housing without noticeable permanent deformation occurring. Due to the fact that strain increases

much more rapidly with stress beyond the yield point for these materials which yield and do not fracture, the overstressed (i.e., beyond yield point) portions of these regions will no longer contribute as much load bearing capability as before the yield threshold was reached. When a significant fraction of material in a given region has been overstressed, permanent deformation becomes noticeable. Therefore, the yield point stress represents a significant threshold for permanent mechanical deformation. The value of yield point stress, designated in this report as s_y , is known for most metals and alloys used in component package construction.

For ceramic materials, there is a large disparity between tensile strength (generally low) and compressive strength (generally high). In ceramic packages where pressure acts on a surface to provide a flexing action (membrane stress), the flexural strength of ceramic materials is analogous to the yield point stress for metals. Flexural strength is determined from the breaking strength of a beam type sample of the material, calculated as if the tensile and compressive stresses increased linearly from zero at the neutral axis to a maximum at the extreme outer fibers.

Using the methods of elasticity theory, briefly reviewed in Appendix 6.1, the general problem faced in our analysis is to determine the stress distribution $s(x,y,z)$ in model structures which resemble the component packages most generally used. These structures are composed of laminar slab elements. Acting on these elements are the applied pressure, P , reaction forces, R , and bending moments, M , as sketched in Figure 2.1 below.

The maximum stress developed at various points in the structure is then set equal to the yield strength or flexural strength as appropriate and the pressure, P , which produces this stress is determined. This is

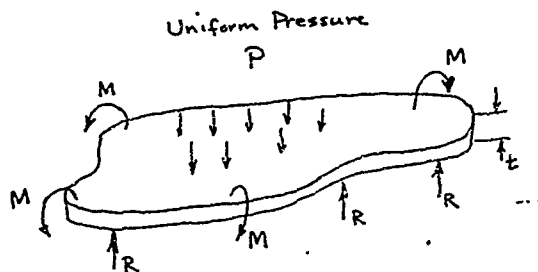


Figure 2.1: Forces and moments applied to laminar slab

converted to an equivalent depth of water and is used to indicate the depth threshold beyond which permanent deformation or fracture can be expected.

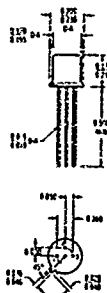
2.2 Mechanical Effects of Pressure on Packages Used for Semiconductor Devices

Contemporary semiconductor devices are housed in a variety of packages. Fortunately, the diversity in package types is not as great as the diversity in device types. Figure 2.2 shows some of the package types used to house discrete transistors. The TO cans are made of metal, with a relatively thin shell cover or cap. Some typical cap thicknesses are given in Table 2.1. Table 2.2 lists typical construction material for caps. The headers (bottom cover) used may vary from relatively thin disks with a thickness not much larger than that of the cap to a relatively massive, thick plate in the case of high dissipation devices, such as power transistors, power zener diodes and gate controlled rectifiers. Some typical header types are shown in Figure 2.3. It should be noted that at least two different materials are used in the construction of each of these headers. Some insulation, usually glass, is used to electrically insulate feedthrough

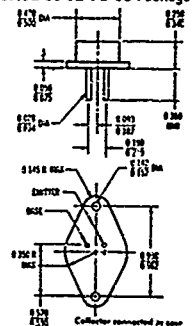
CASE 31 TO-5 Package



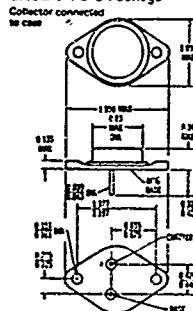
CASE 22 TO-18 Package



CASE 80-02 TO-66 Package



CASE 1 TO-3 Package



CASE 5 TO-36 Package

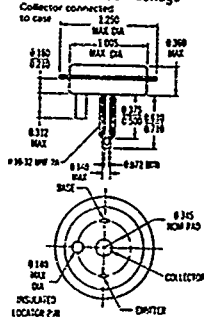


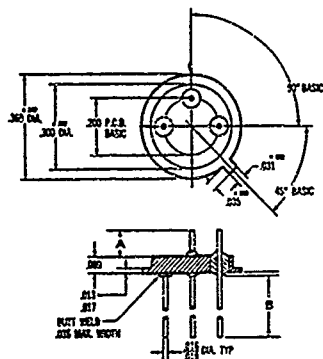
Figure 2.2: Commonly used TO-cans

Table 2.1: Typical dimensions for some TO cans

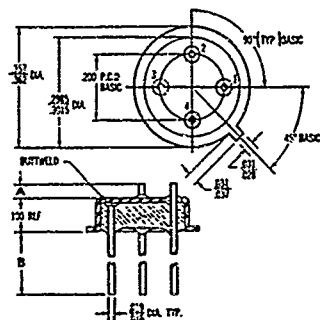
Type	Diameter, in. (2R)	Thickness, in.		Height, in. h
		t_2 (side)	t_1 (top)	
TO-18	0.185	.00775	.0095	.190
TO- 5	0.328	.0115	.0140	.240
TO-66	0.495	.018	.0195	.216
TO- 3	0.800	.019	.0205	.185
TO-36	0.980	.026	.0255	.071

Table 2.2: Typical cap and lip materials and elastic parameters

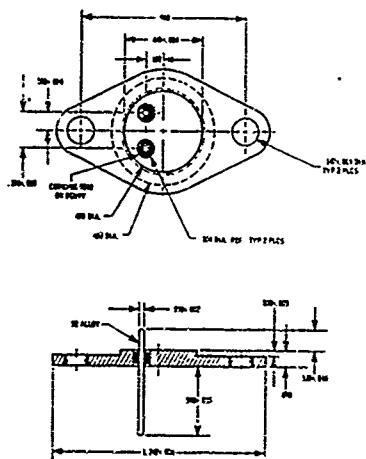
Material	Young's Modulus E (psi)	Poisson Ratio ν	Yield Stress s_y (psi)	Flexural strength s_F (psi)
Kovar	2×10^7	0.28	5×10^4	--
Nickel	2×10^7	0.28	2×10^4	--
Aluminum	1×10^7	0.33	2×10^4	--
Sealing Glass	1.5×10^7	0.25	--	--
Alumina (Alsimag 771)	4.3×10^7	0.22	--	4.4×10^4



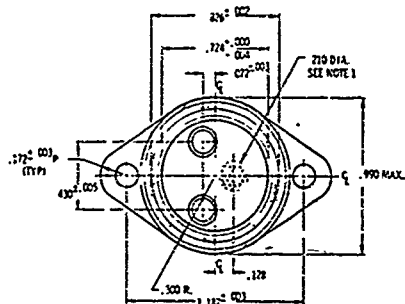
A. Solid TO-5 header



B. Composite TO-5 header



C. TO-66 header



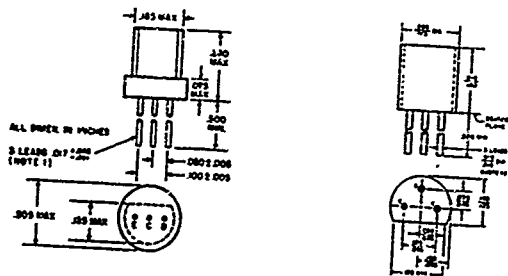
D. TO-3 header

Figure 2.3: Examples of TO-can headers

leads from the metal of the header. In the smaller transistor packages where heat transfer is not a primary consideration, a large fraction of the header material may be a glass, as shown by one of the examples in Figure 2.3.

The TO cans are used for hermetically sealing transistors to prevent the contamination by water vapor and other materials which can interfere with the operation or lead to failure of the transistor, and to provide a known, stable ambient in which operating parameters of the transistor can be specified within guaranteed limits. For those applications where ambient conditions do not require such complete protection for the transistor, the device may be covered with one or more polymeric plastic materials. Typical materials are silicone compounds or epoxies. The physical characteristics of these materials and methods of their application have been discussed by Licari [Ref. 13]. Some typical plastic transistor packages are shown in Figure 2.4.

Aside from hermeticity, there is a significant difference between the TO can type packages and the plastic type packages. The TO can packages have a significant fraction of the enclosed volume as a void occupied only by a gas. On the other hand, the plastic packages allow intimate contact of the package material with the semiconductor element. Thus, when a pressure is applied to a TO can, there is nothing in the interior of the package to resist the pressure and the forces developed on the surface of the can. If these forces are large enough, the can may deform and eventually collapse. On the other hand, a pressure exerted on the surface of an epoxy or a plastic package is transmitted through the plastic directly to the chip. This pressure may be in addition to a pressure which already exists within the plastic package due to such



Plastic Transistor

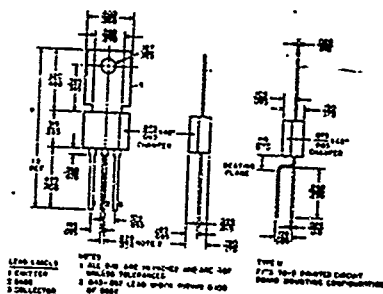
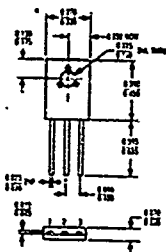


Figure 2.4: Some typical plastic packages for transistors

effects as the differences in thermal expansion coefficient between the plastic and the semiconductor device housed within the plastic and shrinkage during curing operations. Early studies [Refs. 14, 15] have shown that very high mechanical strains may be obtained within a plastic package due to the shrinkage of the plastic following its application at high temperatures. Figure 2.5 shows a plot of stress versus temperature for a plastic package [Ref. 14]. Note that at room temperature, about 25°C, slightly under 4000 lbs/in² is developed by the epoxy package on the device which is contained within it.

Integrated circuit packages come in many varieties also. Figure 2.6 shows some typical examples. Among these are the TO can types, TO-99 and TO-160, which are very similar to the TO-5 packages used for discrete transistors, the flat packs and the dual in-line packages. The dual in-line packages are made both with plastic materials and with ceramic materials. As in the case of the discrete transistors, the plastic dual in-line packages allow the material of the packages to come in intimate contact with a semiconductor device chip. In the case of the TO can type package, the flat pack package and the ceramic package, there is a void inside the package which makes it susceptible to damage by sufficiently high external pressures. For the plastic package, however, forces developed on the outside of the package are transmitted directly through the plastic to the semiconductor device chip.

As was the case with some discrete transistor packages, many different materials are used with each other in various integrated circuit packages. Some of these materials combinations have been discussed by Bower in a review of packaging methods [Ref. 16]. The use of large scale integration in circuits requiring much larger area in chips has led to an increasing size

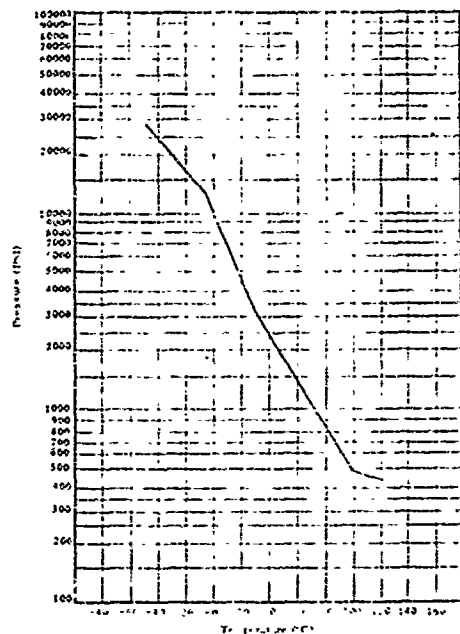
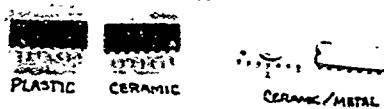


Figure 2.5: Thermal cycling of semi-filled epoxy resin containing embedded pressure transducer [Ref. 14]

IC PACKAGES

DIP



TO CAN



FLAT PACKS

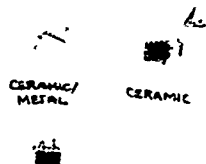


Figure 2.6: Typical IC packages

of packages for these IC's. Also the use of hybrid circuit techniques in which various chips of various different functions are combined and interconnected in one package has led to larger size packages. Figure 2.7 shows some typical packages which are used for LSI and hybrid circuits. These are characterized by relatively large area voids within the package and the use of lids which are relatively thin compared to the dimensions of the void. A descriptive survey of some contemporary LSI packages has been given by Scrupski [Ref. 17].

A convenient starting point in analyzing the effects of pressure on semiconductor packages which contain voids is to use a simple model for the lids of these packages and to apply standard formulas (see Roark [Ref. 12]). Figure 2.8 depicts the structures which are to be used. In the case of a circular disk which is constrained at the edges (rigid side walls) the maximum stress that is developed is in the radial direction at the maximum radial distance, R , with the upper surface in tension and the lower surface in compression. This maximum stress is related to the dimensions and pressure as follows:

$$(\sigma_r)_{\max} = 0.750 \left(\frac{R}{t} \right)^2 P \quad (2.1)$$

In the case of the rectangular cap constrained at the edges, the maximum stress is developed at the center of the long edges and is given by:

$$s_{\max} = P \left(\frac{h}{t} \right)^2 \bar{\epsilon} \quad (2.2)$$

The factor $\bar{\epsilon}$, in Equation (2.2) depends upon the length to width ratio of the rectangular surface, and a table of the values of $\bar{\epsilon}$ as a function of

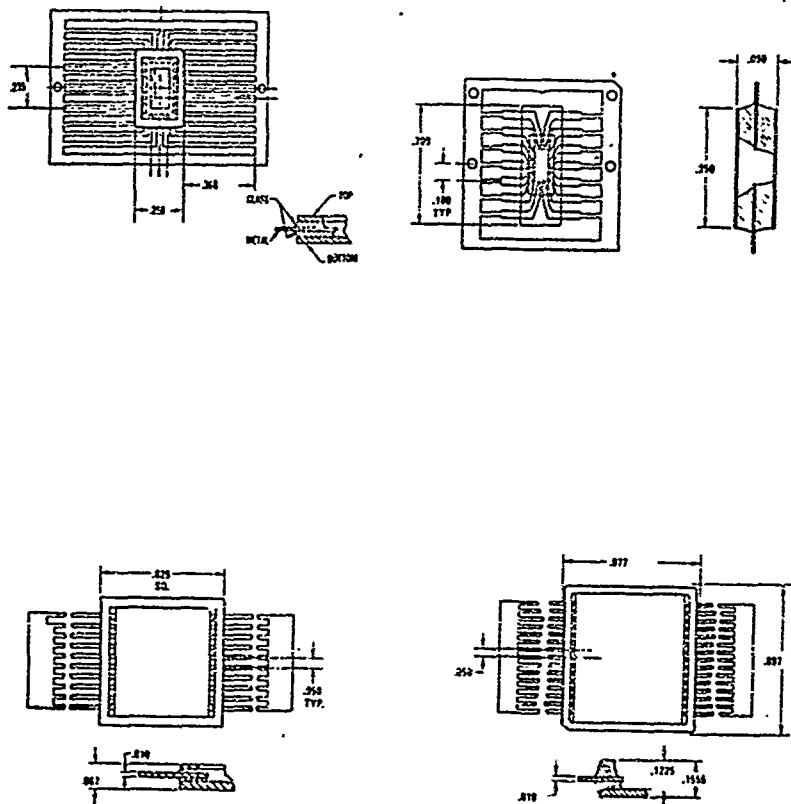
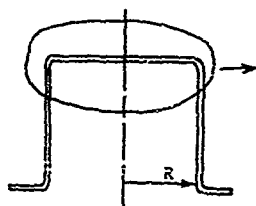
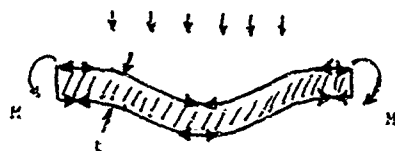


Figure 2.7: Packages for large scale integrated (LSI) circuits

Circular Cap:



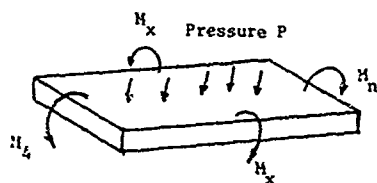
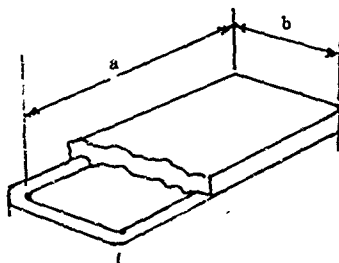
Pressure P



↔ Tensile stress

↔ Compressive stress

Rectangular Cap:



Section through center

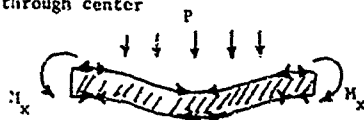


Figure 2.8: Models for circular and rectangular cap stress analysis

this length to width ratio is given in Table 2.3. Using the simple formulas and the relation between depth and pressure for water given by Equation (2.3) below, one may obtain a rough idea of the maximum operating depth for

Table 2.3: Factor β as a function of rectangular cap length to width ratio a/b [Ref. 9]

	1.0	1.2	1.4	1.6	1.8	2.0	∞
β	0.3078	0.3834	0.4356	0.4680	0.4872	0.4974	0.500

various diameter to thickness ratios of disk type package tops, and rectangular top package types. Assuming that the maximum allowable stress is the yield point for the material being used for the tops, values are calculated for typical dimensions and are shown in Table 2.4.

$$h = 2.25 P$$

(2.3)

Although the simple analysis indicates the main factors in the determination of pressure resistance of the top areas of flat packs and of TO cans, it does not include all of the factors which influence the strength of these members, and a more thorough theoretical analysis is required to offer some insight into how the packages actually respond under conditions of external pressure, and also to offer an insight into how packages may be modified to improve the package resistance. Such an analysis for TO cans is given in detail in Appendix 6.2. The results of the analysis for TO cans are given in Table 2.5.

Table 2.4: Maximum operating depths for circular top packages and rectangular top packages calculated from equations (2.1) and (2.2).

Material assumed as shown.

Circular Top Packages

Type	R	t	Material	Maximum Depth (ft)
TO-18	.093	.0095	Kovar	1560
TO- 5	.164	.0140	Kovar	1090
TO-66	.250	.0195	Aluminum	366
TO- 3	.400	.0205	Aluminum	158
TO-36	.490	.0250	Aluminum	162

Rectangular Top Packages

Type	t	a/b	Material	Maximum Depth (ft)
$\frac{1}{4} \times \frac{1}{8}$.005	2.0	Kovar	500
$\frac{1}{4} \times \frac{1}{4}$.005	1.0	Kovar	290
$\frac{3}{8} \times \frac{3}{8}$.010	1.0	Kovar	405

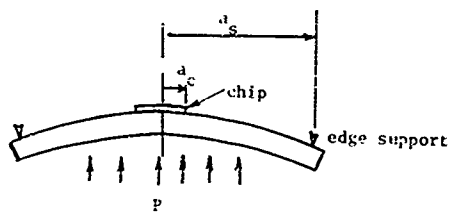
Table 2.5: Comparison of maximum operating depths for some common TO can types with flat tops and with hemispherical tops.

TO-Can Type	Maximum Operating Depth (ft)	
	Flat Top	Hemispherical Top
TO-18	843	7709
TO- 5	550	6500
TO-66	248	2730
TO- 3	92.4	1670
TO-36	114	1870

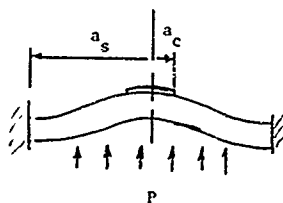
Two situations were modeled. In one, the top of the TO can was assumed perfectly flat. In the other, the top of the can was assumed to be a hemisphere with radius equal to that of the cylindrical wall. The smooth transition provides far less stress amplification in the package material. In actual cases the transitions from sides to top are more or less rounded, giving a situation intermediate between the two extremes considered.

Deformation of the upper cap past the yield point of the material is not desirable, but is not necessarily catastrophic in its effects on device operation, since the cap is not in direct contact with the semiconductor device chip or the lead wires to the chip. It is the bottom cover (header) which is critical in these respects. Deformation of the header may develop stresses in the silicon chip that is bonded to its surface, stresses which exceed the fracture strength of the silicon. This is particularly true when the bonding layer between the chip and the header is capable of transmitting the strain of the upper surface of the header to the lower surface of the chip. Assuming that this situation occurs, we now examine the conditions under which the fracture strength of the silicon chip will be exceeded. To simplify the analysis, the chip will be assumed to have a circular geometry although in practice it is either square or rectangular.

Two extremes can be modeled, as shown in Figure 2.9. In case 1, the circular disc header is supported around the edges by the cap, but the edges are free to flex. In case 2, the circular disc header is effectively clamped by the cap at the edges which does not allow any edge motion. Using both of these models, an analysis is made in detail in Appendix 6.3. Using a model of a coined type (solid metal disc) TO-5



Case 1: edges supported, but not clamped.



Case 2: edges clamped.

Figure 2.9: Header under pressure

Kovar header, 60 mils thick, with a 10 mil thick silicon chip bonded to its surface and the edges supported, but not clamped, the maximum allowable stress will be developed in the silicon at a pressure of 5400 psi (about 12,000 foot depth). Using a model of a header with edges clamped and the same material and dimensions, the maximum allowable stress in the silicon is reached at a pressure of 13,900 psi. This is misleading, however, since the maximum allowable stress in the Kovar will have been reached at about 8900 psi. The calculation does serve to emphasize the reduction in deformation of the center afforded by clamping the edges. Also given in Appendix 6.3 is an analysis of a composite header of Kovar and glass, a combination widely used in both the TO-18 and TO-5 can styles. This analysis indicates that for a typical TO-5 header, the stress developed in a 10 mil thick silicon chip by a pressure of 15,000 psi (33,700 foot depth) will be only about one-half the maximum allowable stress.

Typical flat pack construction is shown in Figure 2.10. The relatively thin lids used with these packages appear to be the most pressure sensitive parts. These may be made of either metal or ceramic. In the latter case, fracture is the most likely mode of failure. An analysis of typical flat pack lids is given in Appendix 6.4. Table 2.6 below gives the result of these calculations assuming Kovar (metal) lids.

Table 2.6: Maximum allowable operating pressures and depths
for some commonly used flat pack styles

Type	a	b	Lid Thickness (in)	Lid Material	P _{max} (psi)	Maximum Depth (ft)
1/4" x 1/8"	.217	.107	.005	Kovar	218	490
1/4" x 1/4"	.180	.180	.0035	Kovar	63	142
			.005	Kovar	129	290
1/4" x 3/8"	.315	.200	.010	Kovar	268	604
3/8" x 3/8"	.300	.300	.010	Kovar	180	405

Another commonly used semiconductor device package is the dual-in-line package (DIP). Some of these resemble the flat pack in the use of a relatively thin metal lid, as shown in Figure 2.11. Another style of DIP, the ceramic DIP is typically constructed as shown in Figure 2.12. The material is usually fairly thick, on the order of 50 mils, above a fairly small cavity, typically 100 to 150 mils in width. Using the structure sketched in Figure 2.12, and assuming that the material is 94 percent Al_2O_3 with a flexural strength of 44,000 psi, the maximum allowable pressure is, for a two to one length to width ratio, using formula (2.2) and Table 2.4,

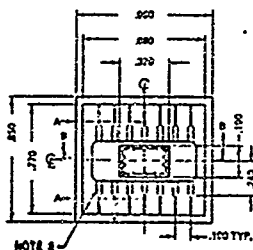
$$P_{\max} = \frac{4.4 \times 10^4}{0.497} \times \left(\frac{0.044}{0.118} \right)^2 = 12,300 \text{ psi},$$

or an equivalent depth of 27,500 feet. As in the case of the flat pack lids, the maximum stress at this pressure is developed at the edge of the cavity at the center of the long dimension.

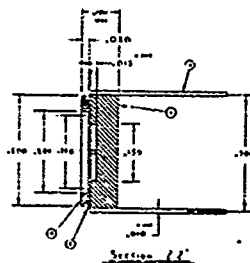
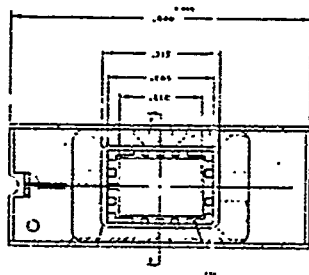
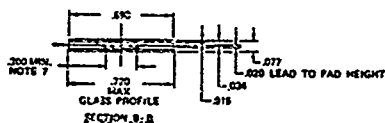
All of the foregoing calculations have been made on idealized models. They provide an estimate of where the package type under consideration will be subjected to stresses in some part of the structure which are above the elastic limit, leading to yielding--in the case of metals--or approaching fracture--in the case of ceramics.

2.3 Passive Component Packages

Passive components (resistors, capacitors, inductors, relays, etc.) come in a great variety of package types. As with transistor packages, the presence of voids causes trouble at sufficiently high pressures. Resistors and capacitors in molded plastic or vitreous encapsulants will generally be



Sylvania Electric Products,
Inc. 14 lead DIP



SCS Corp. 14-lead DIP

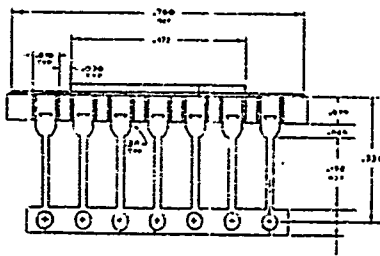


Figure 2.11: Typical Dual-In-Line packages (DIP)
made for metal lids to cover chip cavities

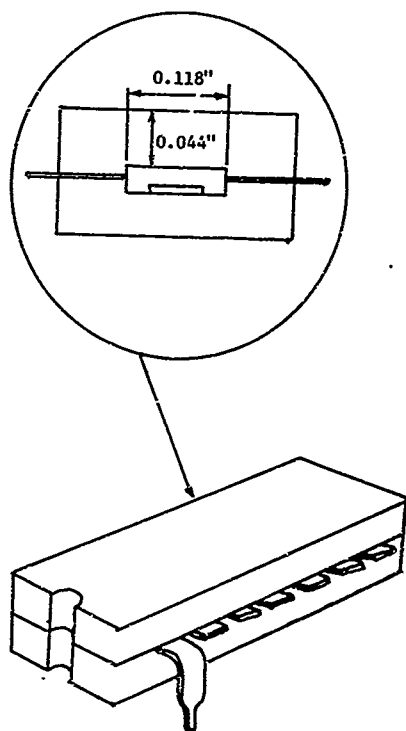


Figure 2.12: Typical ceramic flat pack

able to transmit applied pressure directly to the internal materials that make up the element. Similar remarks apply to potted, open frame chokes or transformers. Some discrete components, however, such as electrolytic capacitors are housed in relatively thin wall packages which contain voids, and are therefore very susceptible to crushing under pressure.

2.3.1 Analysis

Appendix 6.5 gives an analysis of the effects of pressure on the cylindrical package commonly used for many components. As with TO cans, the regions of maximum stress for a given pressure are at the edges where curvature abruptly changes. This suggests that reinforcement in these regions or rounding would give improved pressure resistance.

A typical example, calculated in Appendix 6.5, is for an electrolytic capacitor housing, 1-7/8 inches long x 7/8 inches in diameter made of Al will develop a stress equal to the yield stress in aluminum at an equivalent depth of 800 feet.

2.3.2 Experiment

Only a few limited experiments on passive component packages were performed, to verify previous work by other investigators [Ref. 4] which has provided some basis for assessing the problems in these packages. Although extensive testing was done by Anderson, Gibson and Ramey [Ref. 4], they did not analyze or comment on the data. The only package types in their investigation which correspond to the prototype package analyses given in Section 2.3.1 were cylindrical housings for electrolytic and solid tantalum capacitors. These were usually found to grossly deform and often they had ruptured end seals. This confirms the analysis of Section 2.3.1 which indicates that the greatest stress in the package is developed at the transition from the thin metal cylindrical case to the thick end supports.

2.3.3 Conclusions

Both cylinder and rectangular box type metal housings are very vulnerable to deformation above several hundred psi. Wherever possible these should be replaced by conformal encapsulants (void-free) or filled with an inert liquid to allow pressure compensation.

2.4 Reinforcement or Redesign for Pressure Resistance

In those cases where devices must be kept from contact with the pressure transmission fluid and the existent housings are inadequate for the required operating depth, either reinforcement or a redesigned package must be used.

2.4.1 Analysis

As shown previously in Section 2.2.1, for flat capped TO-type cases, the largest stresses are developed at the periphery of the top where the cylindrical side joins the flat top. Rounding of this shoulder reduces the stress level. A minimum occurs when the cylinder makes a smooth transition to a hemispherical dome. Similar stress level reductions could be expected for gradual transitions on rectangular cross section packages.

Another reinforcement method is to increase the thickness of the material used for the cap. For the curved surfaces, the stress is inversely proportional to the thickness. For flat surfaces, the stress is inversely proportional to the square of the thickness, assuming that in both cases the added material has the same elastic properties as the original material. When the added material has different elastic properties, a more detailed look must be taken at the relation of stress to applied pressure for a given composite structure. An analysis for a composite disc has already been performed in Appendix 6.3. The method can be adapted to gain some insight into how thickening the top of a can with an additional material will improve pressure resistance.

The model used is a circular disc of two different materials with parameters:

	Material 1	Material 2
Young's modulus	E_1	E_2
Poisson's ratio	ν_1	ν_2
Thickness	t_1	t_2

Clamped at the edges and subjected to a pressure p on one side. The force balance condition $\sum F = 0$, equation (6.44) yields the position of the neutral axis (zero strain) as equation (6.45), repeated below

$$z_0 = (A t_2^2 - b_1^2) / 2(A t_2 + t_1) \quad (2.4)$$

where

$$A = E_2(1 - \nu_1) / E_1(1 - \nu_2).$$

Noting that the formula for maximum stress at the edge of a clamped disc, given by Roark [Ref. 10], pg. 217,

$$s_{max} = \frac{3}{8} \left(\frac{R}{t} \right)^2 p \quad (2.5)$$

is independent of material parameters E and ν , the bending moment at the edge can be calculated by assuming a linear strain variation

$$e = \kappa z. \quad (2.6)$$

Then, for the uniform disc

$$M = \int_{-t/2}^{t/2} \frac{3}{2} \left(\frac{R}{t} \right)^2 p z^2 dz = \frac{R^2 p}{8}. \quad (2.7)$$

The same bending moment occurs for the composite disc of the same total thickness and radius. Therefore

$$\frac{R^2 P}{8} = \int_{-(t_2 - z_0)}^{z_0} \frac{E_2 \alpha z^2}{1 - \nu_2} dz + \int_{z_0}^{t_1 + z_0} \frac{E_1 \alpha z^2}{1 - \nu_1} dz. \quad (2.8)$$

This equation is solved to obtain the slope value α

$$\alpha = \frac{3R^2}{8} \{E_2 [z_0^3 + (t_2 - z_0)^3] + E_1 [(t_1 + z_0)^3 - z_0^3]\}^{-1} P. \quad (2.9)$$

2.4.2 Experiment

Experiments were conducted to find a material that would strengthen the housings of semiconductor devices. Several waxes were tried but all failed to add any strength to the housing. Armstrong A-12 epoxy was used to coat two 2N526 transistors. The devices were housed in TO-5 cans. Due to the epoxy having a tendency to run off the side of the can, it was difficult to obtain a uniform coat. The coated transistors were placed in the pressure chamber where a test was conducted. One of the housings failed at 1900 psi and the other one at 4000 psi. Both housings were cut into halves to check the uniformity of the epoxy coating. The header thickness was found to be about the same as the sidewalls. Failure had occurred due to buckling of this thin header in both cases. A mold was fabricated from a 2" x 6" x 0.5" piece of plexiglass. Three holes 7/16" deep and 3/8" deep were drilled into the plexiglass and the mold was cut down the center of the three holes so that the coated housings could be removed. These dimensions allowed molding of a uniform one-sixteenth inch coating over all surfaces of the TO-5 cans housing the devices when the cans were properly held (by the leads) in

the mold cavity. The mold was placed in a vise and all three holes were poured 3/4 full of epoxy and by use of a mechanical manipulator and a three pin socket, three 2N126 transistors were placed in Armstrong A-12 epoxy and allowed to dry overnight. The setup for the molding is as shown in Figure 2.13. After drying at room temperature overnight and then baking for one hour at 90°C, the transistors were placed in the pressure chamber and pressurized in steps of 500 psi. Two of these transistors failed at 4500 psi, the third at 6000 psi. Previous tests had shown that the unsupported housings failed at 1500 psi. Metal thickness was 12 to 14 mils, sides, top and bottom. Therefore, the coating of 62 mils--a factor 4.5 to 5 increase in thickness--provided a factor of three to four increase in pressure resistance. The calculated factor, based on the simple disc model indicated a sixfold increase.

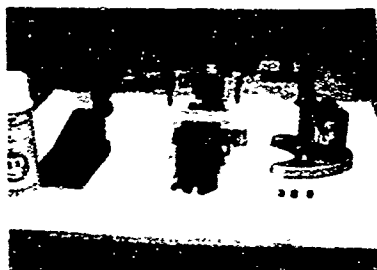


Figure 2.13: Mold and jig for potting transistors for pressure reinforcement.

In a further test, six GE transistors (2N526) designated 213, 256, 383, 234, 238 and 349 were potted using the setup as shown in Figure 2.13. The 213, 256 and 383 units were potted with Shell's EPON(R) ADHESIVE 956. The mixture was 100 parts of A and 58 parts of B (by weight, 10 parts A and 5.8 parts B). The units were cured overnight at room temperature and then baked at 90°C for one hour. CELANESE EPI-RES 510 and EPI-CURE 841 were used for 234, 238 and 349. The mixture was 100 parts of 510 and 22 parts of 841 (10 grams - 510, 2.2 grams - 84). These were cured in the same manner as the three previous transistors. The six transistors were mounted on a circuit board and placed in the pressure chambers where pressure was increased until failure. Figure 2.14 gives the results of the test.

The method of failure in all cases was a collapse of the metal can on the top side. The epoxy on the top adhered strongly during the failure, pulling a plug from top part of the epoxy shell, indicating a shear failure of this material.

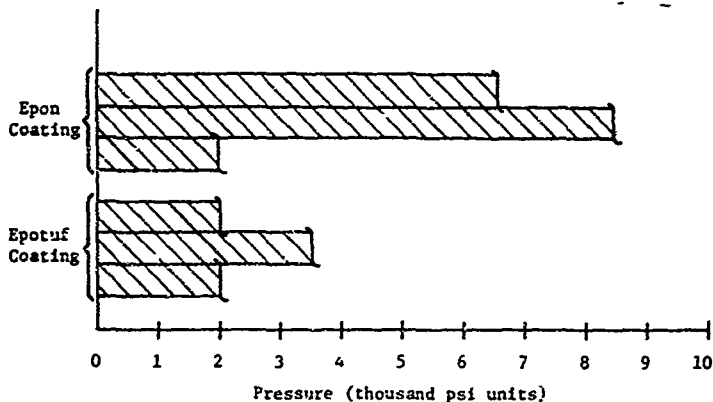


Figure 2.14. Pressure range over which transistors in TO-5 cans potted with epoxy resins functioned. Units failed in next 500 psi increment after curved line.

2.4.3 Conclusions

The use of reinforcement for some transistor packages offers a method of qualifying some devices for operation to moderate depths. The increase in package strength depends upon the thickness and the mechanical properties of the reinforcing material. The possibility of achieving a four to five fold increase in strength has been demonstrated using epoxy. Reinforcement by metallic materials could drastically improve the operating depths.

It should be pointed out that the use of such reinforcement drastically alters the heat transfer properties of the package. Only those devices which are limited heat dissipators are likely to be alterable by reinforcement.

2.5 Composite Material Structures

The construction of semiconductor devices requires the use of many different kinds of materials such as single crystal silicon, polycrystal metal elements and alloys, and amorphous glasses. Added to this problem is one of "built-in" strains induced during fabrication operations. In general, the strain of these materials, measured by their volume deformation $\Delta V/V$, under an applied hydrostatic pressure increment ΔP is different. The compressibility, K , of a material is defined by

$$K = \frac{1}{V} \frac{dV}{dP} \quad (2.10)$$

and is related to the elastic modulus, E , and Poisson's ration, ν , by

$$K = 3(1 - 2\nu)/E \quad (2.11)$$

To a good approximation in the range of pressures to 1000 atmospheres .
(14,700 psi) relation (2.10) can be re-written as

$$\frac{\Delta V}{V} = K \Delta P . \quad (2.12)$$

Consider a structure composed of a "sandwich" of two different materials, material 1 characterized by K_1 , E_1 , and ν_1 , and material 2 characterized by K_2 , E_2 , and ν_2 . Such a structure is sketched in Figure 2.15. Let the parameters α_1 and α_2 represent the respective linear thermal expansion coefficients for the two materials.

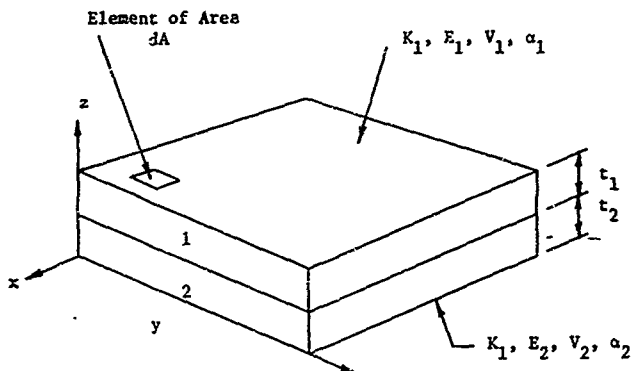


Figure 2.15. Composite material structure.

Suppose that the two materials are subjected to atmospheric pressure, but heated from temperature T_0 to T_1 . If the two materials were not joined, an element of area dA would change to

$$dA_1' = [1 + \alpha_1(T_1 - T_0)]^2 dA \approx [1 + 2\alpha_1(T_1 - T_0)] dA$$

$$dA_2' = [1 + \alpha_2(T_1 - T_0)]^2 dA \approx [1 + 2\alpha_2(T_1 - T_0)] dA$$

where terms in α^2 have been neglected. The expansion ratio is

$$\frac{dA_1'}{dA_2'} = \frac{1 + 2\alpha_1(T_1 - T_0)}{1 + 2\alpha_2(T_1 - T_0)} \quad (2.13)$$

When the two materials are joined, however, and it is assumed that the strains at the interface plane are equal, stresses are set up which tend to deform the structure. A conspicuous example is the bimetallic strip.

When the thickness of one material is much greater than the other, however, the expansion of the thicker material tends to dominate. An example is the growth of an oxide layer (SiO_2) on silicon at about 1100°C , a common step in semiconductor manufacture. Typically the SiO_2 layer is on the order of 1 micrometer thick, whereas the Si may be 200 to 300 times as thick. When the layer is cooled back to room temperature, the larger thermal expansion coefficient of the silicon results in a much larger contraction for the Si than would be experienced by a "free" SiO_2 layer. However, the bonds at the interface transmit the larger strain in the Si, resulting in a "built-in" compressive stress in the SiO_2 . Experimentally, a value of 45,000 psi has been measured in SiO_2 films grown at 1200°C [Ref. 18].

Suppose that the structure is now subjected to a hydrostatic pressure of 1000 atmospheres. The bulk compressibility of Si and SiO_2 are

$$K_{\text{Si}} = 1.05 \times 10^{-6} / \text{atmosphere}$$

$$K_{\text{SiO}_2} = 2.75 \times 10^{-6} / \text{atmosphere}.$$

Analogous to the situation where the thick Si controlled the thin SiO_2 layer, to a good approximation the strain in x and y direction (c.f., Figure 2.15) are both equal to

$$e = \frac{1}{3} K_{\text{Si}} P . \quad (2.14)$$

From elasticity theory for the SiO_2 ,

$$e = \frac{1}{3} K_{\text{SiO}_2} P + \frac{1-\nu}{E} s \quad (2.15)$$

where s is the stress developed in the SiO_2 in the x-y plane due to the difference in compressibilities for the Si and SiO_2 . Substituting the values for SiO_2 for K , ν and E gives

$$s = 6950 \text{ psi (tensile)}.$$

Using the principle of stress superposition, and assuming a "built-in" compressive stress of 45,000 psi in the x-y plane due to the thermal expansion difference, gives a net stress in the SiO_2 layer of

$$s_z = -14,700 \text{ psi}$$

$$s_x = s_y = -(45,000 + 14,700) + 6950$$

$$\text{or } s_x = s_y = -52,750 \text{ psi} .$$

A similar analysis can be applied to the situation where a relatively thin silicon chip (about 10 mils) is bonded to a relatively thick substrate or header (about 60 to 100 mils). For a nickel header, $K_{\text{Ni}} = 4.85 \times 10^{-7}/\text{atm}$. At an applied hydrostatic stress of 1000 atm the difference in compressibility between the Si chip and the Ni base generates a tensile stress

that reduces the x-y stress components in the Si to 680 atm, or 10,000 psi. For a ceramic Al_2O_3 substrate, $K_{\text{Al}_2\text{O}_3} = 4.04 \times 10^{-7}/\text{atm}$. An applied hydrostatic stress of 1000 atm, the difference in compressibility between the Si chip and the Al_2O_3 base, generates a tensile stress that reduces the x-y stress components in the Si to 635 atm, or 9330 psi.

In the case of metallic conductors embedded in glass over the surface of the chip, the thickness dimensions are comparable, making the simplifying assumptions used above inapplicable. Such a situation is shown schematically in Figure 2.16. Since sharp corners may act as stress concentrators, the region in the glass around the relatively sharp corners of the Al strip may be considered critical points. To get an idea of what stress levels might be generated, consider the model sketched in Figure 2.16. The region of glass around the conductor stripe is made symmetrical in the model to facilitate calculation.

The effect of a hydrostatic stress on the model composite structure can be calculated using a finite element model [Ref. 19]. Taking advantage of the symmetry only one quadrant of the structure needs to be considered. This is sketched in Figure 2.17. This quadrant is subdivided into 95 square elements and 2 triangular elements using 119 nodes. The boundary conditions are that for nodes 1 through 7 the displacement in the "1" direction is zero; for the nodes along the "1" axis, displacement in the "2" direction is zero; and along the upper and right side boundaries, a distributed force is applied which is equivalent to 1000 atmospheres of pressure.

The problem was solved assuming a plane strain situation in the direction normal to the plane of the paper. A computer program, ELAS 75,

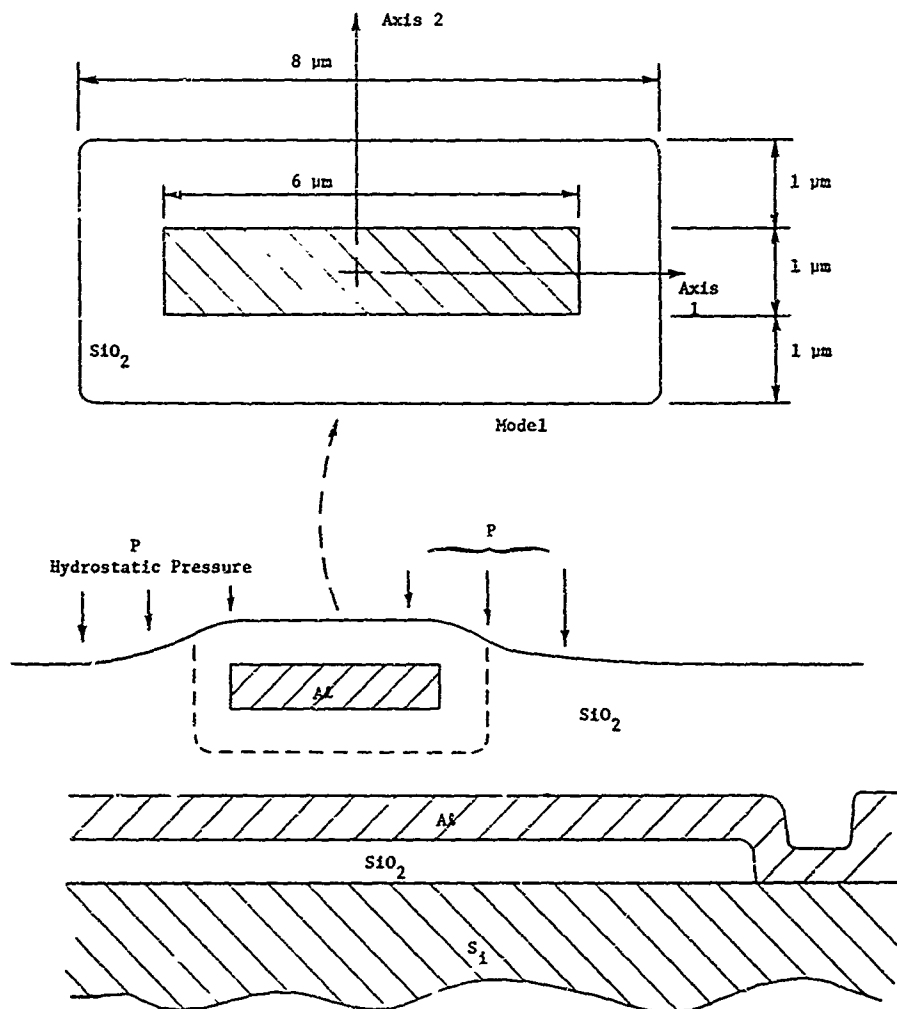


Figure 2.16 Model for Embedded Metallic Conductor in a Multilayer IC Under Hydrostatic Pressure

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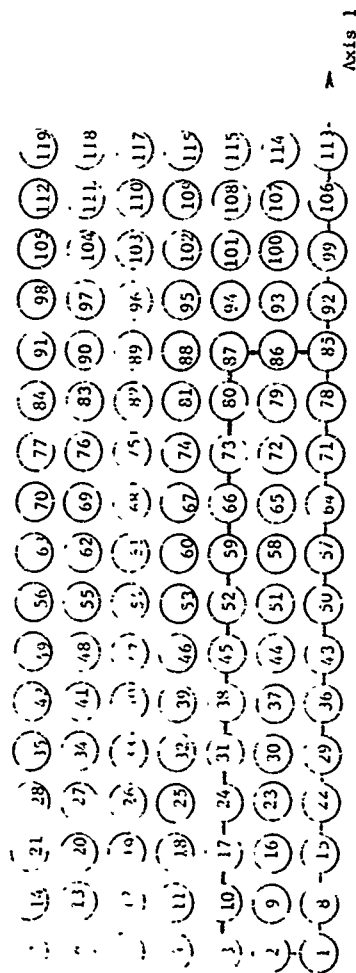


Figure 2.17 Finite Element Model

contained in the Program Library of the Triangle Universities Computation Center (TUCC) facility, was used. The TUCC facility, located in the Research Triangle Park, N.C. employs an IBM 360 Model 145 computer. The ELAS 75 program, in H level Fortran IV language, has been adapted by personnel in the Civil Engineering Department of Duke University from a program developed at the Jet Propulsion Laboratory. The program allows solution of one, two or three dimensional elasticity problems. Input for the program consists of the identification of nodes and their coordinates, identification of elements, specification of boundary conditions and material elastic properties.

Using the model of Figure 2.17, several different situations were examined. These are tabulated in Table 2.7 along with the stress at nodes located in both the glass and the metal at or near the corner. The inclusion of a situation where the interior material provided no support ("sponge") was for the purpose of checking the reasonableness of the answers. Molybdenum was chosen because it is sometimes used (with a gold overlay) in making connector patterns. Also, it represents a harder material, having a modulus of elasticity 4.7 times that of aluminum. The "sponge" material was a fictitious material with an elastic modulus 10 orders of magnitude smaller than that of glass.

An examination of the data of Table 2.7 reveals that aluminum, which has an elastic modulus just slightly larger than that of SiO_2 , will develop slightly higher stress levels near the corner than those in the glass. The maximum stress is about 28 percent higher than the applied hydrostatic stress. Use of a harder material, molybdenum, again results in higher stress levels in the metal than in the glass, with a maximum of 2.13 times the applied hydrostatic stress. When the

interior material yields readily, the stress amplification in the glass is enormous, becoming in one place over 20 times as large as the applied hydrostatic stress.

From the calculations, it can be concluded that the stresses developed in composite glass/metal connector structures used in multilayer integrated circuits will not present any major problems. As with other cases looked at so far, this assumes that there are no voids in the structure and neglects temperature effects during fabrication. The data of Table 2.7 show that a void beneath a glass layer can lead to considerable stress amplification in the glass.

Another composite material structure of practical interest is that of plastic encapsulated devices. The usual construction is to bond the device silicon chip to a metal substrate, which is one of the package connection leads in discrete device construction, or is a tab on the lead frame used with integrated circuit structures. These two cases are sketched in Figure 2.18. Following the chip bond and lead wire bonding from chip to lead frame, the assembly is covered with plastic, typically by a molding operation [Ref. 13]. In this operation, pressures as high as 1000 psi and temperatures as high as 350°F may be used [Ref. 13]. With epoxy, pressures as high as 3000 to 5000 psi may be experienced by the internals of the package due to shrinkage with cooling [Ref. 14]. Silicone resins probably exert less residual pressure due to their much lower thermal expansion coefficients [Ref. 20]. When a hydrostatic pressure is added to the existing "built-in" stress due to molding, the question arises as to whether or not catastrophic or long term failure mechanisms can be initiated, and if so, at what level of applied pressure.

Table 2.7. Stresses developed in a composite structure
under a hydrostatic stress of 1000 atmospheres.
(For node locations, refer to Figure 2.17)

Material 1	Material 2	Node Number	S_1 (atm) (compressive)	S_2 (atm) (compressive)
Glass (SiO_2)	Aluminum	80	865	1045
		87	963	939
		86	1083	830
		80	1200	1083
		87	1277	1240
		86	1130	1160
Glass (SiO_2)	Molybdenum	80	534	1100
		87	1000	922
		86	1220	500
		80	1780	1230
		87	2130	1860
		86	1384	1393
Glass (SiO_2)	"Sponge"	80	8200	1915
		87	9870	15700
		86	1635	20300
		80	~ 0	~ 0
		87	~ 0	~ 0
		86	~ 0	~ 0

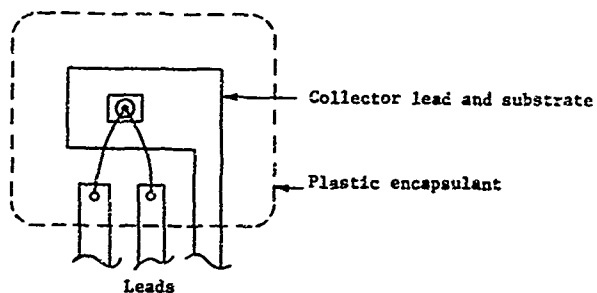


Figure 2.18A Typical Discrete Device Plastic Package

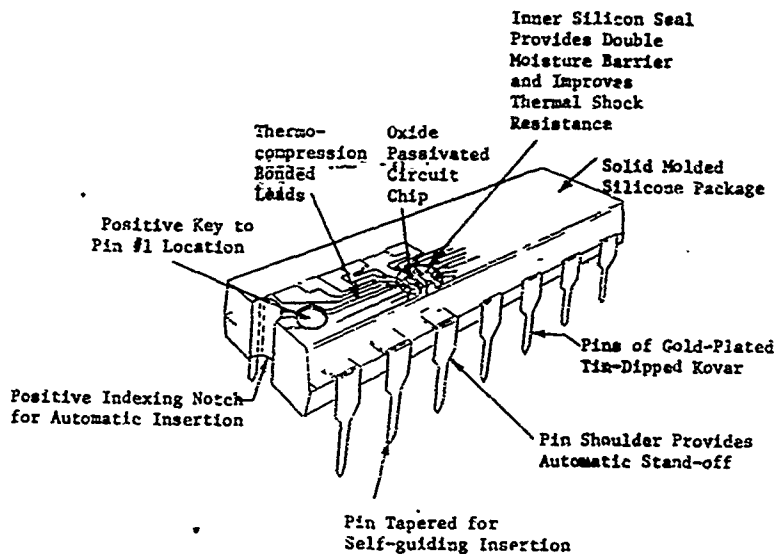


Figure 2.18B Typical Integrated Circuit Plastic Package [Ref. 13]

Although there is a large amount of information on many of the physical properties of various plastics [Ref. 20], data on bulk modulus is not included. It may be estimated from the theoretical relation between the elastic modulus, E , Poisson's ration, ν , and bulk modulus, B [Ref. 11]

$$B = 1/K = E/3(1 - 2\nu). \quad (2.16)$$

However, data on ν is also lacking, and values of elastic modulus depend upon the type of plastic, type of filler used and the degree of filling. In addition, for some of the materials used the elastic modulus values are not available.

Even the compressive strength, which is available for most encapsulating plastics, is of doubtful value as a measure of the deformation under pressure. This is because the method of measurement applies a uniaxial stress rather than a hydrostatic stress.

The lack of data reduces any analysis to a qualitative rather than a quantitative basis. If the plastic material compresses more appreciably than the silicon chip and the metal lead frame material, shear stresses may be set up at the interfaces between different materials. If the plastic tends to adhere strongly to lead wires or the chip metallization, the shrinkage under pressure may be sufficient to pull off lead wires or metallization.

Another type of failure, which has been found to be fairly common [Ref. 6], especially in large area chips such as those used in power transistors and silicon-controlled rectifiers, is the cracking of the chip due to voids in the chip-to-substrate bond. A critical void size can be estimated by assuming that the void is circular, of diameter $2a$,

and that the silicon chip, of thickness t , is constrained by bonding at the edges of the void so that effectively these edges are clamped.

Formula (2.1) can then be applied and manipulated to the form

$$a = t \sqrt{\frac{0.75p}{s}} \quad (2.17)$$

Let a_c denote the critical void radius for a given chip thickness, t , subjected to a maximum pressure of

$$p_{\max} = 14,700 \text{ psi} = 1000 \text{ atm.}$$

Since the maximum allowable stress in silicon is

$$s_{\max} = 3 \times 10^9 \text{ dyne/cm}^2 = 2.96 \times 10^3 \text{ atm,}$$

the critical radius is related to the chip thickness by

$$a_c = 1.99t.$$

A chip thickness of 10 mils requires a 40 mil diameter void beneath it to develop the maximum allowable stress at 1000 atmospheres. This is larger than most small signal transistors, but power transistors may be as large as 150 to 250 mils square, and it is possible that large voids may be developed under such a large chip due to poor quality control of the bonding step of the process.

In addition, the scribe-and-break process used to separate chips processed simultaneously on a silicon wafer can produce mechanical damage along the periphery. Cracks are common and accepted in the MIL-STD-883, Method 2010, Internal Visual (Precap) Inspection, specification if they

meet certain criteria. Figure 2.19 is a reproduction of Figure 2010-5 from Method 2010. Note that if a crack does not point toward an active area, it can be longer than 1 mil. Since a crack can act as a stress concentrator, it is possible that an "acceptable" crack in conjunction with a void can propagate further into the chip under pressure. Further, it is possible for cracks to occur in a chip within active areas and not be detectable by conventional microscopic techniques, or the usual screening procedures of MIL-STD-883. Ordinarily, these hidden flaws would not be harmful. Under applied pressure, however, there may be a conjunction of one or more of these flaws and a bond void which can lead to crack propagation and failure of the device. Therefore, specifying a minimum void size--assuming that such specification can be carried out by an inspection method--may not necessarily assure that no crack propagation will occur. This point needs further study.

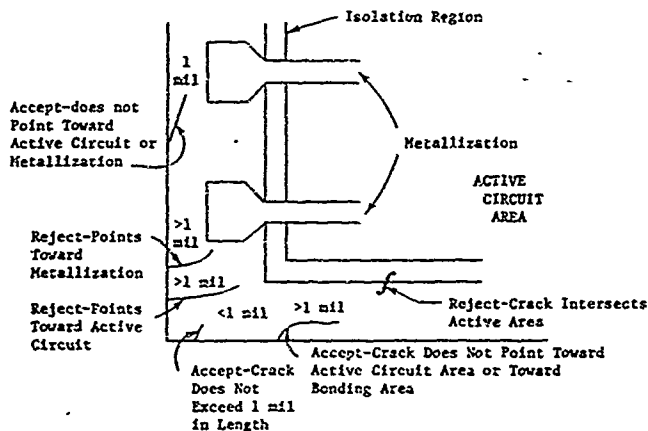


Figure 2.19. Criteria of acceptance or rejection due to peripheral cracks in a device chip
[Method 2010, MIL-STD-883, 1 May 1968]

2.6 Summary

Some simplified approaches have been presented for the analysis of the effects of pressure on various types of component housings used for transistors, integrated circuits and passive components. These analyses enable some rough prediction of the maximum usable depth for these packages. In addition, they provide a basis for extending the analysis to types of packages which have not been explicitly treated. In addition, possible methods have been discussed for package modification and reinforcement to improve pressure resistance.

A mathematical analysis for several composite material structures indicates that no serious problems are expected in discrete or integrated circuit structures operated up to 1000 atmospheres due to differences in material compressibility parameters.

In the discussion of plastic packages which can transmit pressure directly to the chip, it is pointed out that the existence of voids in the chip-to-substrate bond may lead to cracking of the chip if a certain size void is exceeded at a given pressure. More-importantly, it is pointed out that cracks presently allowed in chip inspection methods may be propagated under pressure. A similar conclusion is reached for flaws which may escape the usual precap visual inspection. Such problems will obtain also for chips in direct contact with the pressure transmitting fluid.

3.0 INFLUENCE OF FLUID/PRESSURE ENVIRONMENT ON EXPOSED DEVICE ELEMENTS

3.1 Introduction

In most cases it is not desirable to modify a component package sufficiently to achieve the desired pressure resistance. This may be due to economic factors or to operational factors such as heat transfer limitation. An alternative is to open the package to allow free-flooding by a pressure transmitting dielectric fluid. This introduces two environmental problems which must be considered. First, there is the effect of pressure on the operation of the device. In order to predict what might occur, an understanding of the effects of stress and deformation on the component materials must be developed. Second, there is the effect of ionic contamination on the operation of the device. The possibility of such contamination cannot be overlooked. The seriousness of the problem of ionic contamination of semiconductor devices is well documented. It has led to many improvements in methods of passivation in recent years. In order to predict what levels of ionic contamination will hamper device operation, an understanding of the effects of such contamination must be developed. This chapter deals with these two problem areas for devices exposed to a fluid/pressure environment.

The effects of pressure on semiconductor devices can be analyzed by considering the effects of pressure on bulk material of one conductivity type (either p or n) and the effects of pressure on p-n junctions, since these are the basic building blocks of present day semiconductor devices from diodes to integrated circuits. Fortunately, a great deal of prior work has been done on bulk and p-n junction effects which establishes a basis for understanding how pressure can affect these devices. Another circuit fabrication element, the metal-insulator-semiconductor

(MIS) or semiconductor-insulator-semiconductor (S.S) structure has not been studied, so predictions in this area cannot be made at present.

3.1.1 Analysis of Pressure Effects on Semiconductor Devices

Assume the existence of a stress system, specified in terms of normal stresses S_1 , S_2 and S_3 and shear stresses S_4 , S_5 and S_6 with reference to the cubic cell axes for the diamond type semiconductors silicon and germanium. The notation used is discussed in Appendix 6.1. The effects of these stresses on the resistivity of the semiconductor material can be specified by the piezoresistance coefficients π_{11} , π_{12} and π_{14} [Ref. 21, pp. 38-46]. The usual Ohm's law relation between electric field strength \bar{F} and current density \bar{J} , expressed in component form as

$$\begin{aligned} F_1 &= \rho_0 J_1 \\ F_2 &= \rho_0 J_2 \\ F_3 &= \rho_0 J_3 \end{aligned} \quad (3.1)$$

where ρ_0 is the zero stress resistivity of the crystal, is modified to

$$\begin{aligned} F_1/\rho_0 &= J_1[1 + \pi_{11}S_1 + \pi_{12}(S_2 + S_3)] \\ &\quad + J_2\pi_{44}S_6 + J_3\pi_{44}S_5 \\ F_2/\rho_0 &= J_1\pi_{44}S_6 + J_2[1 + \pi_{11}S_2 + \pi_{12}(S_1 + S_3)] \\ &\quad + J_3\pi_{44}S_4 \\ F_3/\rho_0 &= J_1\pi_{44}S_5 + J_2\pi_{44}S_4 \\ &\quad + J_3[2 + \pi_{11}S_3 + \pi_{12}(S_1 + S_2)]. \end{aligned} \quad (3.2)$$

In the case of uniform hydrostatic stress $S_1 = S_2 = S_3 = P$ and $S_4 = S_5 = S_6 = 0$. The equations (3.2) reduce to

$$\begin{aligned} F_1/\rho_0 &= J_1(1 + \pi_p P) \\ F_2/\rho_0 &= J_2(1 + \pi_p P) \\ F_3/\rho_0 &= J_3(1 + \pi_p P) \end{aligned} \quad (3.3)$$

where

$$\pi_p = \pi_{11} + 2\pi_{12} \quad (3.4)$$

is the "pressure coefficient." Under hydrostatic pressure $\pi_p P$ gives the fractional increase in resistivity of the material.

Values of π_{11} , π_{12} , π_{44} and π_p depend upon conductivity type. Table 3.1 gives values determined experimentally by Smith [Ref. 22]. The effect of doping level on the value of the coefficients is shown in Figure 3.1 which gives a plot of the π_{pq} coefficients versus resistivity for boron doped (p-type) silicon, taken from [Ref. 23]. The values are in units of $10^{-12} \text{ cm}^2/\text{dyne}$, which is equivalent to $6.9 \times 10^{-8} (\text{psi})^{-1}$.

Tufte and Stelzer [Ref. 24] have measured the piezorresistive properties of diffused layers in silicon at surface concentrations ranging from moderately doped material to very heavily doped material (10^{18} per cm^3 to 10^{21} per cm^3 impurity concentration at the surface). They found that in p-type silicon the pressure coefficient π_p was positive and was approximately $6.9 \times 10^{-8} (\text{psi})^{-1}$ to $13.8 \times 10^{-8} (\text{psi})^{-1}$ over the range of surface concentrations investigated. Similarly the value of π_p for n type Si was around $13.8 \times 10^{-8} (\text{psi})^{-1}$ over the range investigated. This behavior is consistent with the data of

Table 3.1. Value of 300°K Piezoresistive Coefficients
(Units 10^{-8} per psi) for Germanium and Silicon Samples
of Various Resistivities. [Ref. 22]

Type, Material, Resistivity (ohm-cm)	π_{11}	π_{12}	π_{44}	π_p
n Ge 5.7	-18.1	-26.9	-944	- 60.7
n Ge 9.9	-32.4	-34.5	-950	- 89.7
n Ge 16.6	-35.9	-37.9	-956	-123.5
p Ge 1.1	-25.5	+22.1	+667	+ 35.9
p Ge 15.0		+34.5	+680	+ 13.1
n Si 11.7	-706	+369	-93.7	+ 39.4
p Si 7.8	+45.5	- 7.6	+953	+ 41.4

Figure 3.1 which shows that as resistivity decreases (higher doping level) the magnitudes of π_{11} and π_{12} both decrease. Since they are of opposite signs, the sum ($\pi_{11} + 2\pi_{12}$) decreases only slowly with decreasing resistivity.

In view of this data and equations (3.3) the following conclusions can be made. For silicon under hydrostatic pressure at 15,000 psi, the fractional change in resistivity will range from about

$$\frac{\Delta\rho}{\rho_0} = 1.5 \times 10^4 \times 13.8 \times 10^{-8} = 0.2\%$$

for heavily doped silicon to about

$$\frac{\Delta\rho}{\rho_0} = 1.5 \times 10^4 \times 40 \times 10^{-8} = 0.6\%$$

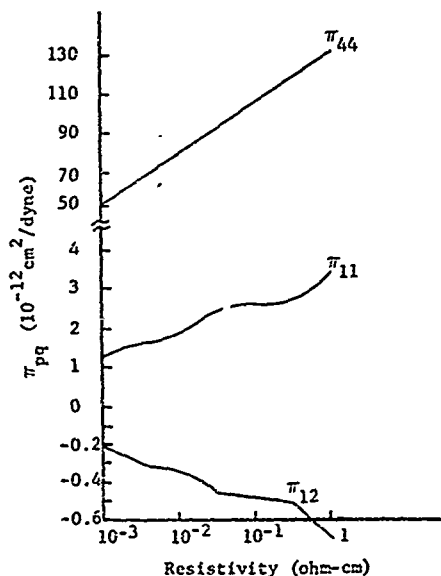


Figure 3.1. Variation of the piezoresistance coefficients as a function of resistivity for boron doped p-type Si at 80°F [Ref. 23].

for lightly doped silicon. For lightly doped germanium the resistivity will decrease by 1 to 2% at 15,000 psi.

When case distortion or the presence of voids creates a stress situation in the semiconductor device which introduces non-hydrostatic stress, particularly shear stress, and at the same time amplifies the stress level, considerably larger changes can be expected in resistivity, as can be seen by comparing the shear stress coefficients π_{44} with the hydrostatic pressure coefficient π_p in Table 3.1. As long as stress can be kept hydrostatic,

however, resistivity changes will remain negligible up to 15,000 psi (greater than 30,000 foot depth).

The effect of stress on p-n junction characteristics has been examined experimentally and theoretically by Wortman and his co-workers [Refn. 25, 26, 27]. The junction current is given by the usual Shockley relation

$$I = I_S [\exp(qV/kT) - 1]. \quad (3.5)$$

However, the usual saturation current expression is modified to the form

$$I_S = I_{p0} \gamma(\epsilon_n) + I_{n0} \gamma(\epsilon_p) \quad (3.6)$$

where I_{n0} and I_{p0} are the zero stress saturation current components. The factor $\gamma(\epsilon)$ depends upon the type of stress (uniaxial or hydrostatic) and the material. For germanium, hydrostatic pressure increases the energy band gap between the [111] conduction band minima and the valence band, leading to a decrease in the minority carrier density with increasing pressure. Silicon, however, has a different conduction band symmetry and hydrostatic pressure decreases the energy band gap, leading to an increase in minority carrier density with increasing pressure. The values for $\gamma(\epsilon)$ for germanium and silicon are shown in Figures 3.2 and 3.3 respectively.

For purposes of illustration of the use of equation (3.5) and the data in Figures 3.2 and 3.3 we assume that a p-n junction is fabricated in a (111) oriented wafer. For a given stress level, the largest effect occurs for a uniform stress covering the total area of the junction. For a uniaxial [111] stress of 15,000 psi applied to a germanium p-n junction will result in about 20% increase in the saturation current value. In contrast, a hydrostatic pressure of the same level will give a negligible change in

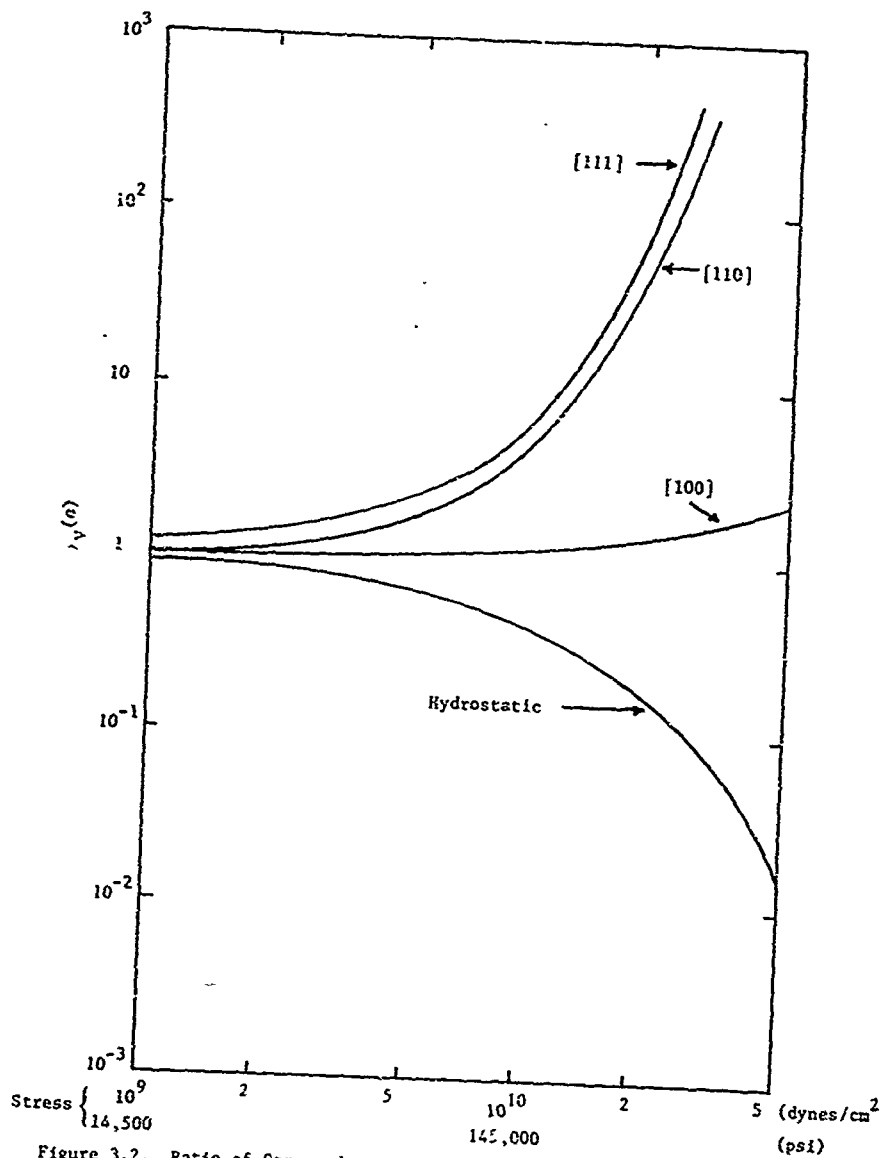


Figure 3.2. Ratio of Stressed to Unstressed Minority Carrier Density for Ce as a Function of Stress for Hydrostatic, [100], [110], and [111] Uniaxial Stress.

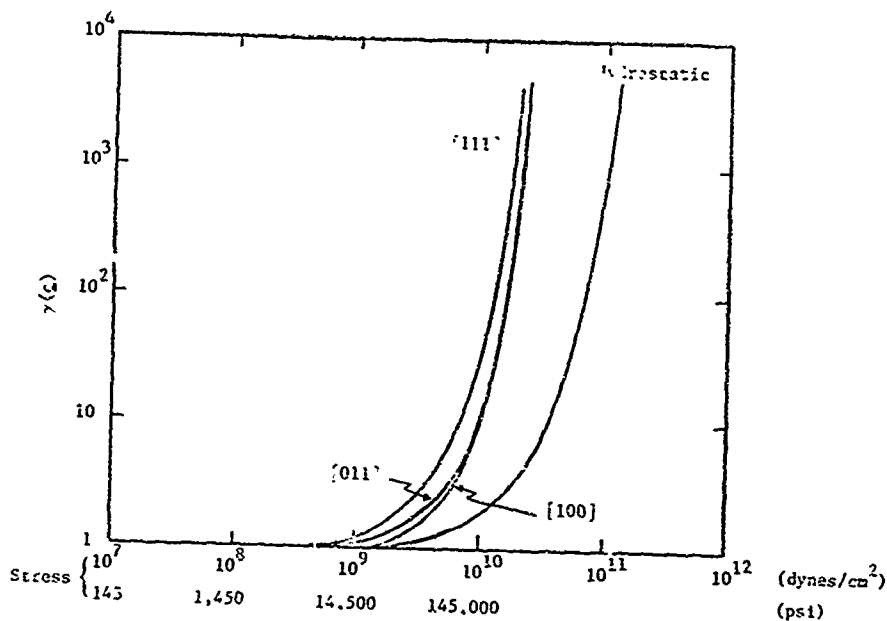


Figure 3.3. Ratio of minority carrier density with stress to the unstressed minority carrier density $\gamma(\epsilon)$ as a function of stress in Si. Values are given for hydrostatic, [100], [111] and [011] uniaxial compression stresses.

saturation current. For silicon (111), stress will give about 25% increase in saturation current, with a negligible change for hydrostatic stress.

To summarize, both piezoresistance and p-n junction effects of planar silicon and germanium device structures under hydrostatic pressure are negligible to at least 15,000 psi. It must be emphasized that these effects are negligible for hydrostatic stresses. For uniaxial stresses, much larger changes in device parameters will occur. These could in many cases lead to device failure in the sense that the device no longer functions in the manner envisioned by the designer. Such a failure mechanism is in many ways more deleterious than outright catastrophic failure because it may lead to operational malfunctions that are difficult to pin down.

3.1.2 Experimental

The theoretical analysis presented in Section 3.1.1 indicated that hydrostatic pressure to 1,000 atmospheres (15,000 psi) should have no effect on the operational characteristics of planar passivated silicon devices or germanium devices. Pressure insensitivity was confirmed experimentally by opening TO cans to expose device chips directly to 10 cc DC200* silicone oil pressured up to 15,000 psi. Both discrete (single transistor) and integrated circuit devices were tested.

Germanium alloy devices, not protected by a passivating oxide or nitride layer as were the silicon devices, were found to be susceptible to moisture in the ambient air and to change characteristics when immersed in DC200. Pressure had no effect on most germanium devices tested, but there was a visible crack in the Ge chip of one Ge alloy power transistor structure. Another was sensitive to mechanical probing, indicating a

* A Dow Corning product

similar problem. This was due most likely to differences in compressibility of the materials used in these structures. Figure 3.4 shows a sketch of a typical germanium alloy structure and indicates the different materials used in the structure.

Silicon planar passivated devices were not affected by exposure to laboratory atmosphere. In addition to devices in de-capped TO-cans some IC devices housed in plastic and ceramic DIP packages were pressure tested. Several devices were tested at the same time by mounting them on a stepping switch in the chamber, as shown in Figure 3.5. The devices tested were:

1. Germanium alloy PNP power transistors, types 2N1412 and 2N1553;
2. Germanium alloy PNP small signal transistors, type 2N526;
3. Silicon planar power transistors, types 2N3740 and 2N4232;
4. Silicon planar bipolar small signal transistors, types 2N2907A (PNP, switch and amplifier) and 2N2222A (NPN, switch and amplifier);
5. Silicon planar MOSFET's, types 2N3976 (N-channel, audio frequency amplifier) and M163 (P-channel, small signal amp);
6. IC operational amplifiers, type 741 with internal frequency compensation, and type 777 with external compensation (both in TO cans and ceramic DIP packages);
7. IC digital circuits, type 7473N (TTL) dual J-K flip-flops in plastic DIP.

The reason for choosing these types to test are as follows:

1. Germanium alloy power transistors 2N1412 and 2N1553 are high power devices, 150 watt and 100 watt dissipation at 25°C case

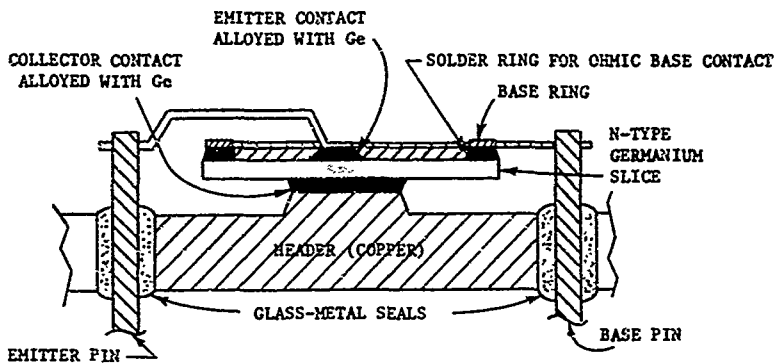


Figure 3.4 Typical construction of germanium alloy power transistor.

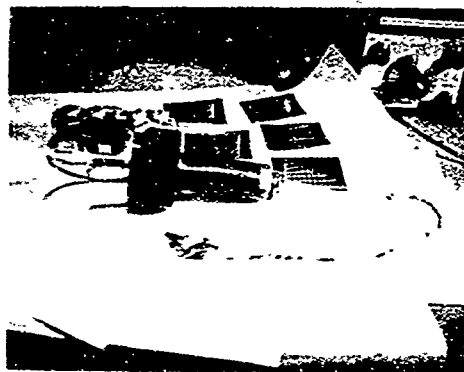


Figure 3.5 Method of mounting devices on stepping switch for pressure test.

temperature, respectively, typical of output transistors used in power amplifier design.

2. Germanium alloy transistors 2N526 are medium power amplifier and low frequency switch devices which have been standardly used in many designs. These are available as a MIL-SPEC JAN type, although the units tested were not JAN type. These are representative of low power Ge alloy devices.
3. Silicon planar power transistors 2N3740 (PNP) and 2N4232 (NPN) are medium power devices, 25 watts and 35 watts at 25°C case temperature, respectively, representative of passivated planar silicon power transistors used in power amplifier design.
4. Silicon planar bipolar transistors types 2N2907A (PNP, switch and small signal amplifier) were chosen as representative of passivated, planar, bipolar silicon transistors used in discrete component circuit design of switching or small signal amplifiers.
5. Type 2N3976, N channel small signal amplifier, was chosen as representative of silicon dioxide passivated, planar MOS field effect transistors.
6. Type 741 is a high performance operational amplifier with internal frequency compensation which is widely used in circuit design, both for analog operations and general feedback applications such as signal amplification and active filters. Type 777 requires external frequency compensation but is representative of "second generation" monolithic operational amplifiers due to its low offset and bias currents and voltages and low noise. Design

features such as latch-up protection and short-circuit protection make the device widely useful.

7. Type SN7473N is a dual J-K flip flop TTL (transistor-transistor-logic) device. It has been routinely used in circuit design for logic and digital signal processing for several years. The circuit configuration makes it typical of a large number of TTL devices which have been widely used.

For the bipolar devices, categories 1 through 4 above, the collector characteristics were observed prior to breaking the hermetic seal, in laboratory air after opening and during immersed operation in the pressure chamber. For the MOSFET's the drain characteristics or the transfer characteristics (I_D vs V_{GS}) were monitored prior to breaking the hermetic seal, in laboratory air after opening and during immersed operation in the pressure chamber. The offset voltage of the operational amplifier, determined by connecting the device in a unity gain (100% negative feedback mode) was monitored for the three different conditions.- It was noted that the offset voltage of the type 741 devices changed with a changing ambient light level. This was no problem in the totally enclosed pressure chamber. This effect was not noted with the type 777 devices but is common to many device tests and must be guarded against. In addition to offset voltage the pulse response and the noise voltage in a unity gain mode were monitored over the range atmospheric to 15,000 psi pressure for the type 777 devices. These had a 33 pf ceramic feedback capacitor for frequency compensation, giving a nominal bandwidth of 1 MHz for the unity gain mode of operation. An HP Model 400H rms VTVM was used to monitor the noise voltage and has a nominal bandwidth of 10 Hz to 4MHz.

A schematic diagram for the circuits used for op-amp testing is shown in Figure 3.6. Figure 3.7 shows a typical pulse response which was the same at atmospheric pressure up to 15,000 psi.

The type SN7473N plastic DIP J-K flip-flop was chosen as a representative TTL structure of widespread utility. Although not available in a TO-can for decapping, the plastic packaging offered a chance to pressure the chip. The test devices, dual J-K flip-flops, were connected as simple scale-of-four dividers counting down clock pulses, as shown in the schematic of Figure 3.8. Minimum voltage of the clock pulse and of the J-K inputs were checked at atmospheric pressure and monitored up to 15,000 psi. Typical input-output waveforms are shown in Figure 3.9.

Table 3.2 presents the results of these pressure tests. The germanium devices were found to be very sensitive to ambient conditions. The silicon devices were found to be insensitive (except to temperature of the ambient, of course) at least on a short-term basis. Only in one case, the TTL digital IC's, was a correlation between pressure and behavior found, which was slight (less than 1% change in enable voltage at the J-K input terminals over the range of 14.7 psi to 15,000 psi).

The results of these tests indicate that pressure effects per se on both Ge and Si devices are negligible. However, because of their lack of passivation the germanium devices are very susceptible to ambient conditions at their surfaces. In addition, the evidence of mechanical damage to two of the Ge alloy power devices tested at high pressures indicates a closer look at the structural design of these devices—but only if extensive use of these devices appears possible in future Navy operating systems.

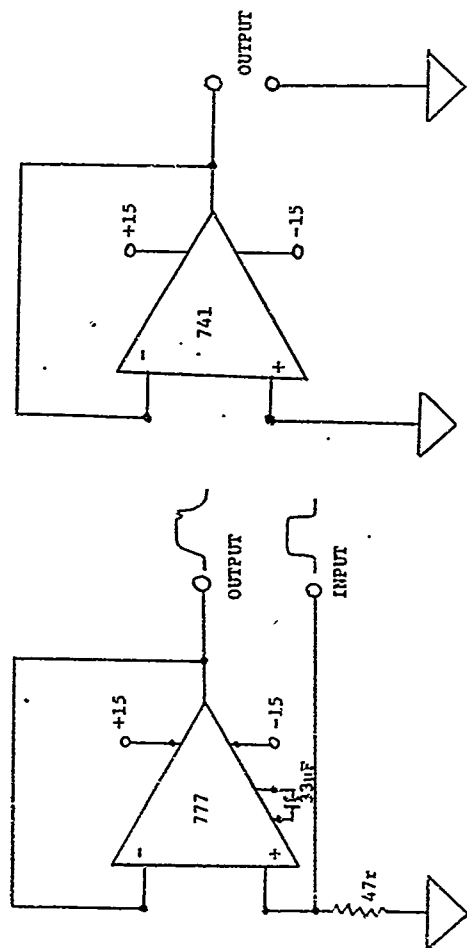


Figure 3.6. Schematic diagrams of test circuits for type 741 and 777 IC op amps

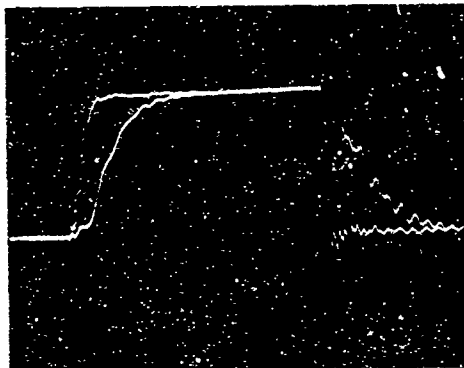


Figure 3.7: Pulse response of type 777 IC op
amp at 15,000 PSI in unity gain mode.

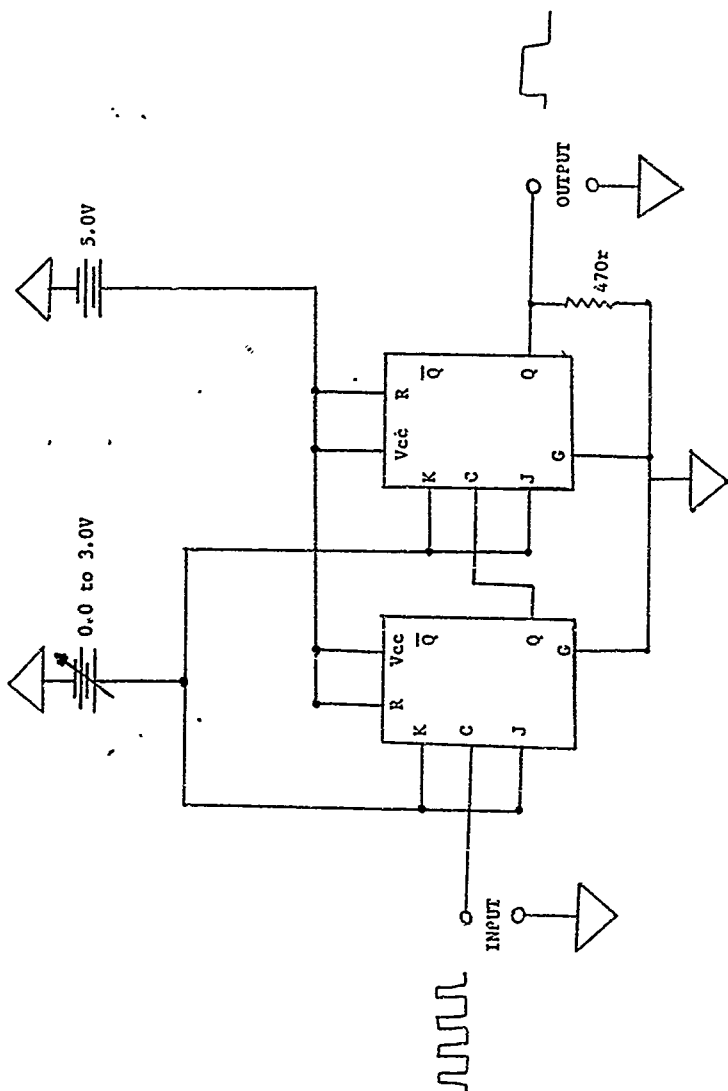


Figure 3.8. Schematic diagram of test circuits for type SN7473N TTL dual J-K flip flops.

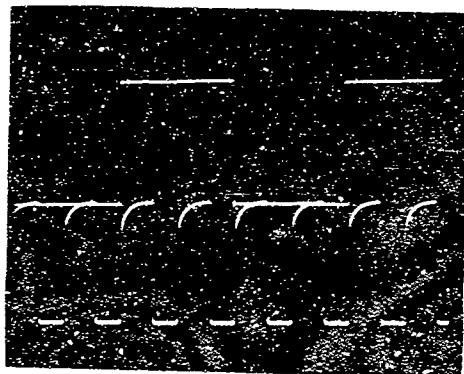


Figure 3.9: Input clock pulse wave form (lower)
and output wave forms from SN743N TTL
dual J-K flip flop at 15,000 PSI.

Table 3.2: Effect of fluid-pressure environment on exposed semiconductor devices

Type	Manufacturer	Description	Behavior upon exposure to laboratory atmosphere	Behavior during pressure tests in DC 200/10cs
2N1412	Motorola	Ge alloy PNP 150 W at 25°C	Large increase in leakage current. Collector I_C vs V_{CE} curves increase slope. Very sensitive to ambient water vapor.	Initial short term improvement in characteristics. Current gain increases. Pressure to 6000 psi and exposure to fluid ambient results in a decrease in output impedance. Changes permanent.
2N1553	Motorola	Ge alloy PNP 106 W at 25°C	Same as above.	Same as above. Some evidence of mechanical damage.
2N526	General Electric	Ge alloy PNP small signal amp and switch	Sensitive to ambient water vapor.	Current gain increases and breakdown voltage decreases. Changes persist. One device covered with Dow-Corning RTV 3144 silicone rubber and operated satisfactorily to 14000 psi.
2N3740	Motorola	Si planar PNP 25 W at 25°C	No change. Device chip covered with polymeric coating by manufacturer.	No change to 12000 psi. Slight reduction in current gain apparent due to better cooling.
2N4232	Motorola	Si planar NPN 35 W at 25°C	Same as above.	Same as above.
2N2907A	Motorola	Si planar PNP small signal amp and switch	No change, except one device appeared to be slightly sensitive to ambient moisture.	No change to at least 14000 psi. Slight reduction in gain due to better cooling.
2N2222A	Motorola	Si planar NPN small signal amp	No change.	Same as above.

Table 3.2 (Continued)

Type	Manufacturer	Description	Behavior upon exposure to laboratory atmosphere	Behavior during pressure tests in DC 200/10c.s.
2N3796	Motorola	Si planar MOS FET, N channel, small signal amp	No change.	No change to at least 15000 psi.
·M163	Silliconix	Si planar MOSFET No change. P channel, small signal amp	No change.	Same as above.
μ507741393	Fairchild	Si planar IC op amp with internal freq. compensation	Offset voltage sensitive to ambient light.	Offset voltage constant to at least 15000 psi.
SG777GT	Silicon General	Silicon planar IC No change. op amp - needs external frequency compensation	No change.	Pulse response and noise voltage in unity gain mode not affected by pressure to 15000 psi. Some change noted in offset voltage, but not specifically related to pressure.
μ6A777393	Fairchild	Same as above except in ceramic DIP	N/A	Same as above.
SN7473N	Texas Instruments	Silicon planar IC TTL-dual J-K flip-flop in plastic DIP	N/A	At constant clock pulse amplitude (3.0 volts) the minimum voltage for firing on J-K inputs decreased slightly with pressure.

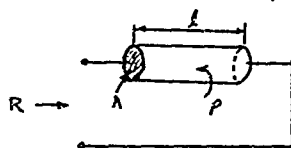
3.1.3 Conclusions

The experimental results presented in Section 3.1.2 confirm the theoretical analysis of Section 3.1.1. Pressure to 15,000 psi, per se, does not harm planar silicon or germanium devices. Damage may occur on non-planar structures due to material compressibility mis-matches. Direct immersion of germanium devices in a pressure transmitting fluid generally results in a change in operating characteristic due to factors discussed below in Section 3.3. However, this is a contamination effect, not a pressure effect.

3.2 Passive Components in a Fluid/Pressure Environment

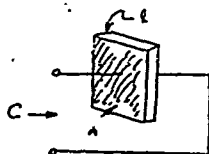
3.2.1 Effects of Pressure

The application of pressure to electrical circuit passive components can be expected to influence the behavior in two ways: through changes in dimension due to mechanical strain and through changes in material properties. An illustration is afforded by considering the models sketched below.



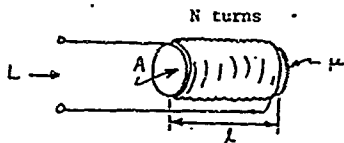
Prototype Resistor

$$R = \rho l / A$$



Prototype Capacitor

$$C = \epsilon A / l$$



Prototype Inductor

$$L = \mu N^2 A / l$$

Figure 3.10: Prototype models for passive components

The changes in parameter values due to a pressure change ΔP can be written as

$$\Delta R = \left(\frac{\epsilon}{A}\right) \frac{d\epsilon}{dP} \Delta P + \epsilon \frac{d(\epsilon/A)}{dP} \Delta P \quad (3.7)$$

$$\Delta C = \left(\frac{A}{\epsilon}\right) \frac{d\epsilon}{dP} \Delta P + \epsilon \frac{d(A/\epsilon)}{dP} \Delta P \quad (3.8)$$

$$\Delta L = \left(\frac{N^2 A}{\epsilon}\right) \frac{d\epsilon}{dP} \Delta P + \mu N^2 \frac{d(A/\epsilon)}{dP} \Delta P. \quad (3.9)$$

In each case, the first term represents a change due to a change in material electromagnetic properties with pressure and the second term represents a change due to a change in dimension with pressure.

The change in dimension can be expanded as

$$\frac{d}{dP} (A, \epsilon) = \frac{1}{\epsilon} \frac{dA}{dP} - \frac{A}{\epsilon^2} \frac{d\epsilon}{dP} = \frac{A}{\epsilon} \left[\frac{dA/dP}{A} - \frac{d\epsilon/dP}{\epsilon} \right]. \quad (3.10)$$

The change in area with pressure can be expressed for a circular cross section as

$$\frac{1}{A} \frac{dA}{dP} = \frac{\pi}{\pi r^2} \frac{d(r^2)}{dP} = \frac{2\pi r}{\pi r^2} \frac{dr}{dP} = 2 \frac{dr/dP}{r}. \quad (3.11)$$

The fractional changes in linear dimensions, $(dr/dP)/r$ and $(d\epsilon/dP)/\epsilon$, are related to material bulk compressibility, K_v , by

$$\frac{1}{r} \frac{dr}{dP} = \frac{1}{\epsilon} \frac{d\epsilon}{dP} = -K_v/3. \quad (3.12)$$

Therefore,

$$\frac{d}{dP} (A/\epsilon) = -\frac{K_v}{3} (A/\epsilon). \quad (3.13)$$

Similarly,

$$\frac{d}{dP} (l/A) = \frac{l}{A} \left[\frac{dl/dP}{l} - \frac{dA/dP}{A} \right] = \frac{K_v}{3} (l/A). \quad (3.14)$$

These results show that the dimensional changes due to pressure tend to decrease capacitance and inductance and increase resistance by an amount proportional to the compressibility of the core material. An important exception is the case where foil electrodes may not be completely tightly wound. In this case, the effect of pressure is to narrow the spacing and thus increase the capacitance.

To obtain an idea of the order of magnitude of these effects, some typical numerical values can be considered. For steel, $K_v/3$ is approximately $1.5 \times 10^{-8} (\text{psi})^{-1}$. At 15000 psi the change in inductance of a steel core, due to dimensional changes only, would be about

$$\left(\frac{\Delta L}{L} \right)_{\text{dimensional}} = 1.5 \times 10^{-8} \times 15000 = 2.25 \times 10^{-4}$$

or about 0.2%. For a resistor with a core material of graphite with a resinous binder, a typical compressibility could be approximated by taking that for a plastic material such as nylon, for which $K_v/3$ is approximately $1.2 \times 10^{-6} (\text{psi})^{-1}$. Using this, at 15000 psi

$$\left(\frac{\Delta R}{R} \right)_{\text{dimensional}} = 1.2 \times 10^{-6} \times 1.5 \times 10^4 = 1.8 \times 10^{-2}$$

or about 2%. A similar order of magnitude would be expected for capacitors using a polymeric material such as mylar as a dielectric spacer. In electrolytic capacitors which rely on a thin oxide film as the dielectric, the

relatively small compressibility of the film would be expected to contribute a negligible change in capacitance.

Changes in the electromagnetic parameters ρ , ϵ , and μ will occur with pressure. A relatively large change in ρ occurs in carbon composition resistors. The core material consists of a suspension of carbon particles in a resinous binder. Increasing pressure increases the effective contact area of the carbon granules, decreasing the bulk resistivity of the core. This effect predominates over the increase in resistance due to dimensional changes to give an appreciable net decrease of resistance with increasing pressure, observed by many experimenters. For film type resistors, the order of magnitude change of ρ with P can be estimated by considering some of the data of Bridgman, shown in Figure 3.11 below.

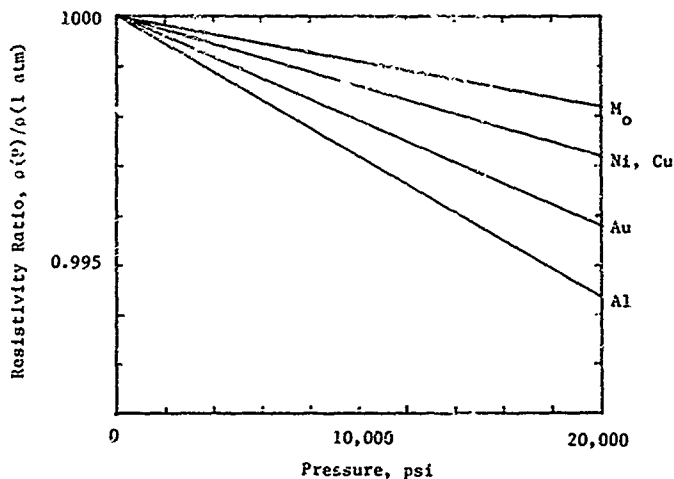


Figure 3.11: Effect of pressure on resistivity of several metallic elements

Changes in ϵ with pressure have been studied for a limited number of solids. Mayberg [Ref. 28] has studied the change in dielectric constant with pressure for alkali halides and MnO, all materials with cubic symmetry. Some of his data is given below in Table 3.3.

Table 3.3. Change of Dielectric Constant, ϵ_r , with Pressure P for Alkali Halides and MnO. [Ref. 28].

Material	Temp. ($^{\circ}$ C)	Average, $-\frac{\partial \ln \epsilon_r}{\partial P}$ (atm^{-1})
MnO	30	0.32×10^{-5}
LiF	28 - 29	0.45×10^{-5}
NaCl	25 - 30	0.99×10^{-5}
KCl	28 - 29	1.06×10^{-5}
KBr	26	1.19×10^{-5}

At 1000 atmospheres (roughly 15000 psi) the change in ϵ_r is on the order of 1% or less for these materials. Published data is sparse, or non-existent, for the effect of pressure on ϵ_r for polymeric materials. Some insight is offered by considering the data obtained for liquids and making an extrapolation from this.

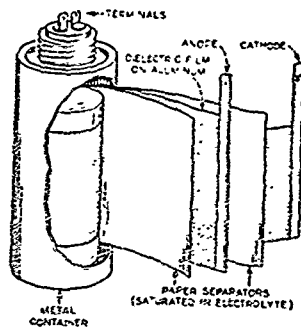
For non-polar liquids, the dielectric constant increases slowly with pressure. For n-pentane an increase in pressure from 1 atmosphere to 1000 atmospheres would give about 5% increase in dielectric constant. For polar liquids also the dielectric constant increases with pressure at low frequencies, although for high frequencies (several hundred KHz) and for high pressure (several thousand atmospheres), the dielectric constant can

eventually start to decrease with increasing pressure [Ref. 29]. It has also been reported that the vitreous form of phenolphthalein and phenol-formaldehyde resin exhibit a decrease in dielectric constant with increasing pressure [Ref. 29].

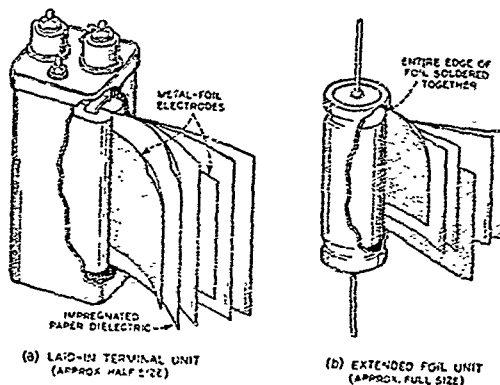
In reviewing this behavior, it appears that capacitors which use a not-too-viscous liquid dielectric, such as the impregnated paper capacitors shown in Figure 3.12, will increase their capacitance up to a few percent at 1000 atmospheres. On the other hand, polymeric dielectrics of high molecular complexity can be expected to exhibit a slight decrease in capacitance to dielectric changes.

The permeability, μ , of a magnetic material depends upon the magnetization M induced by an applied magnetic field, H . The maximum value of M , the saturation magnetization, M_s , and the Curie temperature, T_c , i.e., the temperature at which M_s drops to zero, has been found to generally decrease in Fe-Ni alloys, although the magnitude of the decrease is dependent upon the composition, as shown in Figure 3.13, taken from [Ref. 30]. It is well known that application of a magnetizing force to a ferromagnetic material can result in a mechanical strain $\delta l/l$. The magnitude and sign (+ or -) of this magnetostrictive effect depend upon the relative orientation of the magnetization with the strain. This strain is equivalent to an external stress applied to the material. A reciprocal relation also applies: mechanical stress can influence the magnetization. Thermodynamic reasoning leads to a relation [Ref. 31]

$$\left(\frac{\partial M}{\partial S}\right)_H = \frac{1}{T} \left(\frac{\partial T}{\partial H}\right)_C \quad (3.15)$$



Electrolytic capacitor.



Paper capacitors in hermetically sealed housings.

Figure 3.12: Typical internal construction for paper and aluminum foil electrolytic capacitors

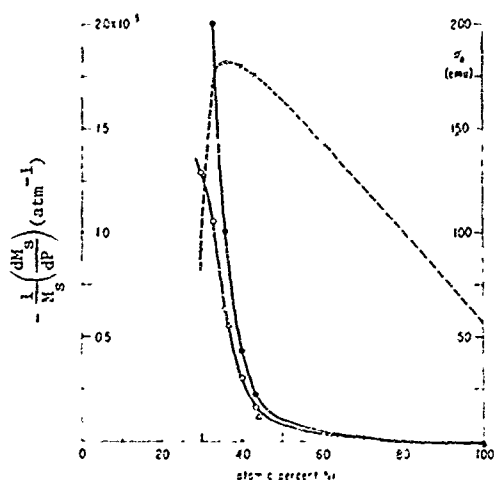


Figure 3.13A: Rate of change of saturation magnetization, M_S , with pressure as a function of composition in Ni-Fe alloys [Ref. 30]

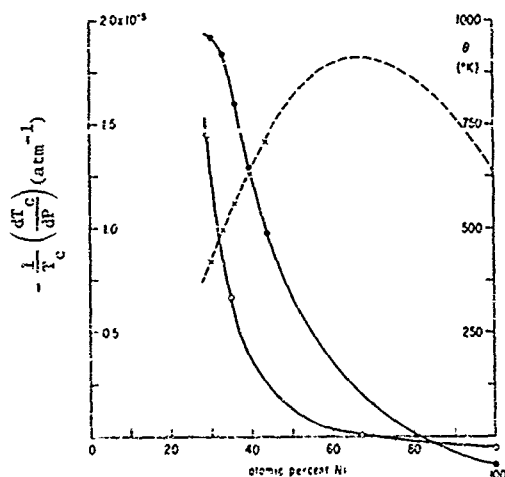
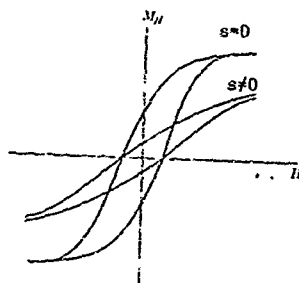


Figure 3.13B: Rate of change of Curie temperature T_C with pressure as a function of composition in Ni-Fe alloys [Ref. 30]

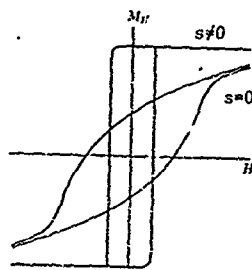
between the change in magnetization with stress, at constant field H , and the change in strain with applied field at constant stress [Ref. 31]. Application of a uniaxial stress can have a marked effect on the induced magnetization for a given H field, as shown in two examples in Figure 3.14 [Ref. 31]. These effects are attributable presumably to the existence of a favorable magnetic orientation axis (due to minimization of the free energy). Orientation of this axis with respect to the stress direction determines the direction of shift of the magnetization versus field curve. In one case shown, Permalloy with 68% Ni, application of a tensile force shifts the M_H vs. H curve so that a given value of M_H is achieved with a smaller field strength H . In the case of Ni, a tensile force increases the value of H required to achieve a given M_H . In both cases there is a noticeable shift in saturation magnetization.

Application of hydrostatic pressure to a polycrystalline ferromagnetic material would not introduce a unique stress axis. Hence, the marked shift of M_H vs. H which occurs for uniaxial stress would not be expected to occur. The relatively small shift in saturation magnetization with pressure of Fe-Ni alloys, shown in Figure 3.13, supports this reasoning. The largest value is $\sim 1 - 2\%$ at 1000 atmospheres. Based upon this, it is expected that the change in permeability of laminated steel cores used in chokes and transformers will remain negligible up to 15000 psi. Powdered cores, on the other hand, may increase effective permeability significantly due to denser packing under pressure.

Another passive circuit element frequently used in electronic circuits is the coaxial cable, modeled in Figure 3.15. For this circuit element, the inductance per unit length and capacitance per unit length are given by



A. Effect of tension on hysteresis loop of nickel.



B. Typical hysteresis loop of Permalloy with 68% Ni with and without applied tension.

Figure 3.14: Effect of uniaxial stress on two different ferromagnetic materials [Ref. 26]

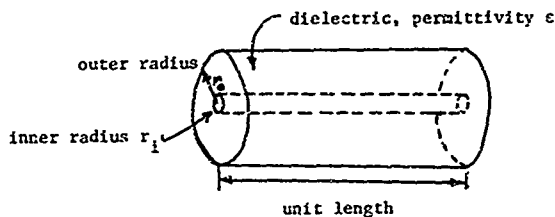


Figure 3.15: Coaxial cable model.

$$L = 2 \times 10^{-7} \ln(r_o/r_i) \quad \text{hy/m} \quad (3.16)$$

$$C = \frac{55.6 \epsilon_r}{\ln(r_o/r_i)} \quad \text{pf/m} \quad (3.17)$$

The effect of hydrostatic pressure would be to compress the dielectric material, typically polyethylene or teflon, to a much larger extent than the metallic inner conductor, so that to a good approximation r_i would remain constant. The resulting changes in inductance and capacitance would be

$$\frac{\Delta L}{L} = \frac{1}{\ln(r_o/r_i)} \frac{d(r_o/r_i)}{dP} \Delta P \quad (3.18)$$

$$\frac{\Delta C}{C} = \left[\frac{1}{\epsilon_r} \frac{d\epsilon_r}{dP} - \frac{1}{\ln(r_o/r_i)} \frac{d(r_o/r_i)}{dP} \right] \Delta P. \quad (3.19)$$

Since $dr_o/dP < 0$, the inductance per unit length would decrease with pressure. The capacitance could either decrease, increase, or remain relatively constant, depending on the relative sizes of the two terms in square brackets. Propagation delay and characteristic impedance, defined by

$$\tau = \sqrt{LC} = \sqrt{\mu\epsilon} \text{ sec/m} \quad (3.20)$$

$$Z = \sqrt{L/C} = \sqrt{\frac{\mu\epsilon}{4\pi^2}} \ln(r_o/r_i) \quad (3.21)$$

would also be only slightly affected at 1000 atmospheres. Taking as an example a section of RG-S8A/U cable with polyethylene dielectric, the changes which could be expected at 1000 atmospheres can be calculated. For polyethylene, the linear compressibility is about 0.011 per 1000 atmospheres. Therefore, for $\Delta P = 1000$ atmospheres, 14,700 psi,

$$\frac{1}{r_o} \frac{dr_o}{dP} \Delta P \approx -0.011 .$$

The value of r_o/r_i for RG-S8A/U is about 3.0, which gives

$$\frac{\Delta L}{L} = - \frac{0.011}{\ln 3} \approx -0.01$$

$$\frac{\Delta C}{C} = + \frac{0.011}{\ln 3} + \frac{1}{\epsilon_r} \frac{d\epsilon_r}{dP} \Delta P .$$

The change in dielectric constant should be negligible at 1000 atmospheres. Therefore, the inductance per unit length decreases by about 1 percent and the capacitance per unit length increases by about 1 percent. Delay time

r should be negligibly affected, and the characteristic impedance will be decreased by about 1 percent.

3.2.2 Fluid Effects

In those cases where component housings would crush at pressures well below those desired for operation, the housing must be pressure compensated. Two types of problems can result--changes in operation due to the presence of a fluid of higher dielectric constant, i.e., oil rather than air, and changes due to contamination. Except for the air dielectric variable capacitor, the presence of a higher dielectric fluid will probably not significantly change the electrical operating characteristics of the immersed circuits. Contamination, however, must be carefully considered.

As shown in Figure 3.12, paper capacitors are constructed with an impregnating fluid in the paper spacing the metal foil electrodes. The impregnant may be a wax, oil, or synthetic material such as chlorinated naphthalene or chlorinated diphenyl [Ref. 32]. If the case has an aperture to allow free passage of the pressure transmission fluid--say, for example, silicone oil--the effect of long term contact of the oil with the capacitor impregnant must be known in order to assess the possibility of deleterious reactions of the generation of contaminants which could be transported to contamination sensitive components. A similar consideration applies to aluminum foil electrolytic capacitors, which use an aqueous solution of ammonium borate, boric acid, and glycol, or similar electrolyte solutions [Ref. 32]. Typical construction of an aluminum foil electrolytic capacitor is shown in Figure 3.12 also.

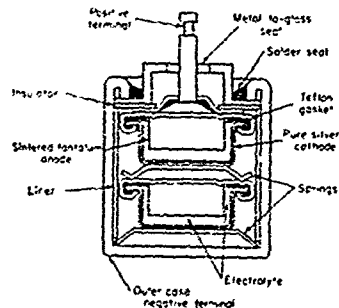
Another type of electrolytic capacitor, the tantalum type, is extensively used in circuit construction. Typical construction for the "wet" types and for the solid electrolyte types of tantalum capacitors is shown

in Figure 3.16. The "wet" types use sulfuric acid or aqueous lithium chloride as the electrolyte because of the high conductivity required to reduce series resistance [Ref. 32]. The miniature-type tantalum-pellet capacitor is inherently pressure compensated if the electrolyte completely fills the interior of the case. The dual cell type shown could possibly be compensated by having its outer case punctured to allow oil to fill the voids around the interior capacitor cells, assuming that these are completely filled by liquid electrolyte. The solid electrolyte (MnO_2) tantalum capacitor, if of the construction shown, would require an interior liquid fill for pressure compensation. The liquid would have to be inert to the electrolyte. Pure silicone oil would probably fulfill this requirement, but the presence of any polar liquid contaminant could change the value of capacitance if transported through the oil and accumulated at the capacitor. Experimental work on the effects of water, methanol, and isopropyl alcohol on MnO_2 solid electrolyte capacitors has shown that these polar liquids can cause an increase of capacitance and of leakage current [Ref. 33]. In this work the capacitors were uncased and immersed in the liquids. However, exposure to room air at 50% R.H. also gave an increase in capacitance of about 6% over a period of 30 minutes. There may be some shifts due to water vapor in the oil.

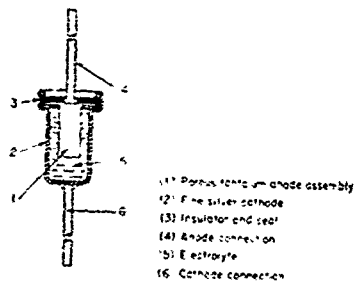
Immersed operation of transformers and chokes in oil should introduce no problems providing that the insulation materials are not soluble or softened to the point where turns could be shorted under pressure.

3.2.3 Experiment

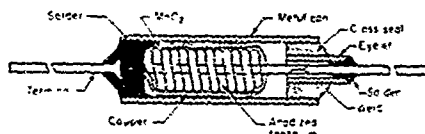
Passive components have not been tested so far in this investigation. This was due to the fact that past work by other investigators had yielded a fair amount of data on passive components but a limited amount on semi-



A. Construction of a two-cell hermetically sealed tantalum-pellet electrolytic capacitor



B. Construction of miniature-type tantalum-pellet electrolytic capacitor



C. Construction of a solid-electrolyte tantalum capacitor.

Figure 3.16: Typical tantalum electrolytic capacitor construction

[Ref. 32]

conductor devices. The most comprehensive passive component pressure testing reported has been undertaken by Anderson, Gibson and Ramey [Ref. 4]. These investigators used twenty component test sets taken in 1000 psi increments to 10,000 psi and then back to atmospheric pressure. The results of these tests can be summarized as follows:

1. Resistors:

- a. Carbon composition resistors in molded cases showed a consistent decrease of resistance, R , with pressure, although occasional units exhibited an increase in R before decreasing at higher pressures. The decrease was uniform with pressure for many units. Other units decreased rapidly for the first few thousand psi and then decreased at a lower rate to 10,000 psi. Those in hermetically sealed cases showed little change to 3,000 - 4,000 psi and then abruptly decreased to about 0.9 the initial resistance.
- b. Film resistors, both carbon and metal, showed little or no change with pressure. Metal oxide films showed somewhat more change, but less than 10% at 10,000 psi.
- c. Wirewound resistors in molded cases showed some change, with occasional units exceeding 10%, but less than 50%. One unit exceeded a 50% change. Wirewound resistors in metal cases exhibited abrupt decreases to 50%, apparently due to case deformation onto the spool.

2. Capacitors:

- a. Ceramic capacitors generally showed less than 10% change (some increased, some decreased in value) although occasional units exhibited a 10 - 50% change. A significant fraction (30 -

35%) of ceramic capacitors in phenolic cases had a greater than 50% change.

b. Paper-mylar and solid impregnated capacitor changed very little (a few percent at most) with pressure, with one unit excepted, which had a 10 to 50% change over the 10,000 psi pressure interval.

c. Mica and glass-foil capacitors generally changed only a few percent, although some glass-type units had a change between 10 and 50 percent.

d. Aluminum foil electrolytic capacitors exhibited erratic changes with pressure, with 10 to 50% variations typical. Metal cases were deformed and frequently found to be displaced from the end seals.

e. Solid tantalum capacitors showed less than 10% change on one batch, although generally the change was 10 to 50%, with several greater than 50%, and many of the metal cases were deformed and had ruptured end seals.

3. Inductors:

a. R.F. chokes (air core) showed generally less than 10% change, although one unit varied 10 to 50% from its initial value.

b. Audio chokes (steel core) generally changed less than 10%, although in one batch four out of six exhibited a permanent change of greater than 50%.

4. Transformers:

a. Of twenty R.F. transformers on ceramic forms, half showed less than 10% change while half varied 10 to 50%.

b. Several batches of audio transformers were tested. The open frame type generally showed less than 10% change in transforma-

tion ratio with a few exceptions. Epoxy molded types usually showed larger changes, 10 to 50%, with several units exhibiting permanent changes of greater than 50%.

3.2.4 Conclusions

The theoretical analysis of Section 3.2.1 indicates that many materials used for passive component construction exhibit little change in parameter values with pressure to 15,000 psi. This includes the materials used in:

1. wirewound resistors
2. film resistors
3. capacitor dielectric materials (except air)
4. laminated ferroelectric cores for inductors and transformers.

Fabrication materials with appreciable void content are likely to exhibit large changes in parameter values with increasing applied pressure. These include:

1. composition resistor material
2. ferrites
3. powdered cores.

For the first group of component materials, the use of molded or vitreous encapsulants without voids, which are capable of transmitting stress directly to the internals should provide devices which are relatively stress insensitive. The second group of materials must either be protected from stress, or their change in parameter values must be known and compensated for in some manner if they are to be used.

These conclusions are generally supported by the experimental evidence cited in Section 3.2.3.

3.3 Semiconductor Components Exposed to a Contaminated Fluid


Transistors and other semiconductor devices are housed in packages to protect them from mechanical damage. In addition, however, many of these devices must have a hermetic seal to prevent the accumulation on or near the device of ionic contaminants and water vapor. From long experience, it has been found that such contamination can seriously interfere and often lead to catastrophic failure of semiconductor devices. We now examine the problems which may occur when a semiconductor device is deliberately exposed to a fluid under pressure which may possibly contain ionic contaminants and water vapor.

3.3.1 Ionic and Water Vapor Contamination Effects on Devices

It has been long known that ambient conditions have a marked effect on transistor performance. Brown [Ref. 34] reported on the formation of conducting "channels" on the surface of the base region of grown junction npn germanium transistors. This was attributed to the inversion of the conductivity type of the surface of the base region from p-type to n-type due to the presence of charges on the surface from an unspecified source.

A subsequent study by Kingston [Ref. 35] reported the formation of n-type channels on p-type base region of a grown junction germanium transistor due to absorbed water vapor. A review by Kingston [Ref. 36] of surface phenomena on germanium, citing the work of many experimenters, revealed that the type and density of induced charge carriers at the surface of germanium is independent of the bulk resistivity of the germanium. The type of charge carrier induced at the surface depends only upon the nature of the ambient. Table 3.4 shows the relation between various gas ambients and surface conductivity type as given in [Ref. 36]. In

Table 3.4: Surface conductivity type and surface potential due to various gas ambients [Ref. 36]

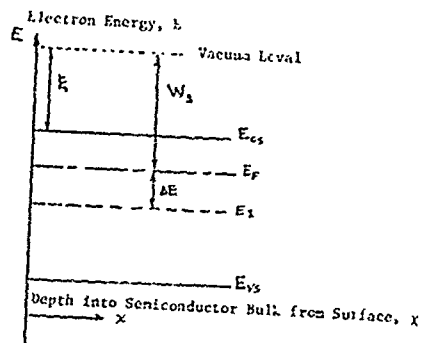
<u>Gas</u>	<u>Surface conductivity type and potential</u>	
$H_2O + N_2$	n type	V_s positive
$H_2O + \text{air}$		
$H_2 + O_2$		
N_2 (dry)		
Air (dry)		
O_2 (dry)		
H_2O_2		
O_3	p type	V_s negative

addition to these studies directed towards a theoretical understanding of the effects, practical studies were made of the effects of various ambient conditions on transistor reliability [Ref. 37]. Both O_2 gas and water vapor were found to have a large effect on the reverse saturation current, junction breakdown voltage, and the current gain of both npn and pnp alloy junction germanium transistors.

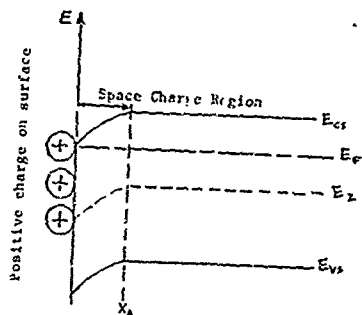
The effect of water vapor is pertinent to the present study. Water vapor in contact with pnp alloy junction germanium transistors [Ref. 37]. was found to: (1) decrease collector base junction breakdown voltage, V_B ; (2) decrease the reverse saturation current, I_S , until a high vapor pressure was reached; then I_S increased rapidly; (3) increase the forward current transfer ratio, α (and, therefore, β , since $\beta = \frac{\alpha}{1-\alpha}$). This effect of water vapor was found to be similar to the effect of positive ions on transistor surfaces, and essentially the same results were found for freshly etched surfaces on the structures as well as for units kept under bias in oxygen for two weeks after etching.

Sensitivity to ambient conditions of germanium devices is understandable, since under normal conditions of surface preparation, these devices have only a thin layer, 10 to 50 angstroms, of native oxide covering the bulk germanium. This thin insulating layer allows ionic charges which accumulate on the outer surface of the oxide to exert strong electrostatic attraction on free charge carriers in the bulk. The effects of such attractive forces can be summarized by considering the diagrams in Figure 3.17.

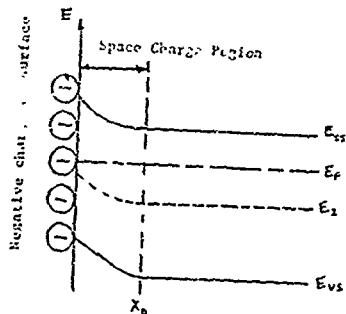
Ideally, there is no disturbance of allowed and forbidden energy levels as an electron approaches the surface ($X = 0$ in the diagrams of Figure 3.17). Figure 3.17A depicts this ideal situation for an n-type semiconductor. On



A. "Flat Band"
Condition - no charges
on surface.



B. Positive charge on
surface induces an accu-
mulation layer of electrons
adjacent to surface,
width x_a .



C. Negative charge on
surface repels electrons
deeper into bulk, creating
a depletion layer, width
 x_d .

Figure 3.17: Effects of surface charges on semiconductor energy bands.

this diagram, we denote the edge of the conduction band by E_{CS} , we denote the upper edge of the valence band by E_{VS} , we denote the intrinsic Fermi level by E_i . This is the energy level for which the probability of electron occupation is exactly 1/2 in intrinsic material, that is, in not intentionally doped material. Because of the deliberate addition of donor-type impurities to make this model material n-type, the Fermi level is now moved upward to a position denoted by E_F displaced by an amount ΔE from the intrinsic Fermi level, E_i . The energy difference between the Fermi level, E_F , and the vacuum level--that is, that energy at which an electron is free of the material but has zero kinetic energy--is called the work function of the material and is here symbolized by W_S . The energy difference between the bottom of the conduction band and the vacuum level is denoted by ξ and is called the electron affinity of the material. Vertically we plot a scale of electron energy, and the horizontal scale represents depth into the semiconductor bulk from the surface, which we will denote by x . This is the ideal situation. The density of free carrier electrons in the conduction band is given by Equation 3.22 below:

$$n = n_i \exp (\Delta E) . \quad (3.22)$$

The density of holes in the valence band is given by Equation 3.23 below:

$$p = n_i \exp (-\Delta E) . \quad (3.23)$$

In both of these equations, the energy difference, ΔE , is given by Equation 3.24 below:

$$\Delta E = (E_F - E_i) / kT . \quad (3.24)$$

In Figure 3.17B, we depict a situation in which positive charge has somehow accumulated on the surface of the semiconductor. The effect of this accumulation is to attract free electrons in the bulk toward the surface of the semiconductor and hold them there by electrostatic attraction. Now this represents a dynamic situation with electrons continually coming to and leaving the surface, but there is always a net of electrons attracted to the surface due to the accumulated fixed positive charge on the surface. The effect of the accumulation of electrons near the surface is to bend the allowed energy bands as shown in the diagram. Note that the spacing between the Fermi level, E_F , and the intrinsic Fermi level, E_i , has now increased to account for the increase in concentration of electrons near the surface. We denote the level of the distance into the material over which the energy bands are disturbed from their ideal position shown in Figure 3.17A by X_A . It is possible, with sufficient positive charge on the surface, to accumulate a large concentration of electrons in the germanium just underneath the surface, and when this happens, we call it an accumulation layer. In other words, an accumulation of carriers of the same type as the doping of the bulk germanium. Figure 3.17C shows another situation which might occur. In this situation, an accumulation of negative charge on the surface of the semiconductor induces a higher concentration of holes, or positive-charged carriers, from the semiconductor bulk. These holes tend to decrease electron concentration at the surface. If the number of holes attracted toward the surface is sufficiently large, the electron-hole concentrations may be essentially balanced. By definition, the surface is intrinsic, and the separation between E_F and E_i is zero. If sufficient negative charge accumulates adjacent to the semiconductor surface, the

conductivity type may be changed from n- to p-type, in which case the surface is said to be "inverted."

To summarize, charges which accumulate on the surface of a semiconductor may influence the electronic properties of the semiconductor surface. Charge of like sign as the majority carriers in the semiconductor will tend to repel these carriers and attract minority carriers. Charge of opposite sign to that of the majority carriers will tend to cause an accumulation of majority carriers near the surface.

Figure 3.18 shows the situation which occurs for the energy levels of a semiconductor when a real oxide layer is present on the semiconductor surface. In this figure, the presence of the oxide has introduced some energy states which serve to trap charge and to change the band structure at the surface of the semiconductor. In the situation shown here in Figure 3.18, we have an n-type semiconductor with an oxide layer on it; the thickness of the oxide layer is given by x_0 , and the disturbance of the oxide layer and interfacing with the semiconductor has created some energy states which are shown as rectangles on the diagram. The energy states which are immediately at the interface between the oxide and the semiconductor, colored dark, are called fast surface states; and energy states which are located in the bulk of the oxide or at the surface of the oxide adjacent to the gas ambient are called slow surface states. The reason for these designations is that charges or charge carriers from the bulk of the semiconductor may rapidly come to equilibrium with the interface states or fast states so that a change in electrostatic attraction at the surface of the semiconductor can cause these states to come to equilibrium in one microsecond or less. These states occur in a density

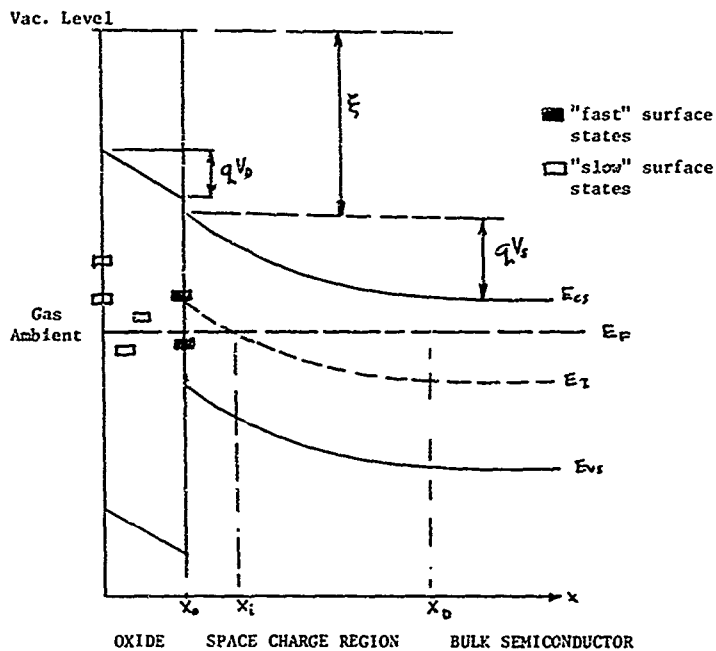


Figure 3.18: Energy diagram of an oxide layer on a semiconductor.

of about $10^{11}/\text{cm}^2$ for germanium and of about $10^{12}/\text{cm}^2$ for silicon [Ref. 38, page 357]. Since these states lie at the interface [Ref. 38, page 348], they are insensitive to changes in the ambient conditions—that is, the ambient gas conditions—at the surface of the oxide. The slow states, which are shown by the open rectangles on the diagram, take much longer to come to equilibrium with carriers from the bulk. These states may require as long as seconds or longer to come to equilibrium. They are associated with either states in the oxide bulk or on the surface, which may possibly be adsorbed species [Ref. 38, page 348]. The density of the slow states varies with the way in which the oxide has been formed on the semiconductor, but the lower limit of these states is equivalent to about $10^{13}/\text{cm}^2$ [Ref. 38, page 358]. If the oxide is thin, as is the case with a native oxide (formed at temperatures of a few hundred degrees Kelvin at most) on germanium and silicon, the presence of slow states caused by adsorbed gaseous species can cause instabilities in device parameters as the ambient changes.

The situation shown in Figure 3.18 shows the bands bending upward near the surface of the semiconductor at the semiconductor-oxide interface. This situation implies that there is an accumulation of negative charge in the fast and in the slow states or a net accumulation of negative charge in these states which serves to attract holes toward the surface of the semiconductor at the oxide-semiconductor interface; and in this situation, we have shown an inversion region between x_0 and x_1 . In other words, the fixed charge in the oxide and at the interface has accumulated sufficient holes to completely invert the surface on n-type germanium to p-type. In the depth in the semiconductor between x_1 and x_d , the material gradually changes from intrinsic to n-type again, and in this region there is a lower density of electrons, free charge carriers, than there is in the bulk of

the n-type semiconductor so this region is referred to as a depletion region. The total region between x_0 and x_d is termed a space charge region, and into the semiconductor beyond x_d the semiconductor behaves as it would ideally with no disturbance on its surface. In other words, the semiconductor exhibits its bulk properties.

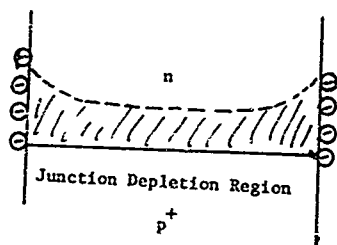
The change in breakdown voltage, V_B , of a p-n junction has been explained by Garrett and Brattain [Ref. 39] in terms of surface charge near the p-n junction which alters the electric field pattern in the junction region near the surface. The model by these authors to explain the experimental results they and others had obtained is shown in Figure 3.19 in terms of a p^+-n junction structure (p^+ means a heavily doped p-type region).

In Figure 3.19A, a situation is shown in which positive charge has accumulated near the p-n junction; the positive charge has accumulated on the surface of the semiconductor. Shown shaded is the junction depletion region. The accumulated positive charge is shown as $+$. Note that the accumulation of positive charge at the junction serves to attract more electrons to the surface and the more lightly doped n-type material which causes a narrowing of the junction depletion region near the surface. This narrowing can lead to a decrease in the breakdown voltage of V_B . Formation of a depletion region or an inversion region, as shown in Figure 3.19B, due to the accumulation of negative charge on the surface near the junction widens out the junction near the surface and results in an increase in V_B towards the ideal bulk breakdown value.

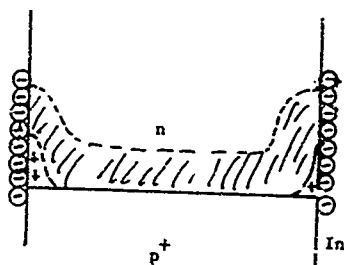
The formation of a channel (inversion region), as shown in Figure 3.19C, results in an increase in effective junction area which can increase the reverse saturation current. This will be discussed in more detail later.



A. Positive charge near junction



B. Small negative charge layer near junction



C. Large negative charge layer near junction inverting part of the n-type surface

Figure 3.19: Model of Garrett and Brattain [Ref. 39] used to explain the dependence of p^+-n junction breakdown voltage, V_B , upon ambient conditions.

In addition to pointing out the desirability of channel formation to increase V_B , the analysis of [Ref. 39] also revealed that surrounding the junction by a material of high dielectric constant would help to increase V_B .

With the advent of silicon planar, diffused device technology, the possibility of using relatively thick layers of SiO_2 , an amorphous, high quality insulator, became apparent. These could be grown on the device surface in an oxidizing atmosphere at temperatures near 1000°C during the diffusion process. The ability of these "thermal" SiO_2 layers to provide stable operating characteristics for silicon devices was reported by Atalla, et al [Ref. 40]. A range of thicknesses from thin ($150\text{--}300 \text{ \AA}$) to thick ($4,000 \text{ \AA}$) was used. With surfaces protected in this manner, the silicon devices were found to exhibit stable characteristics, at least on a short-term basis, when exposed to a variety of different ambient conditions such as wet N_2 gas, wet O_2 gas, dry N_2 and O_2 , ammonia, and ozone. Junctions with thin oxides ($150\text{--}300 \text{ \AA}$) stored in room air in plastic boxes for 15 months were reported to have showed no change in characteristics.

A subsequent report by Atalla and other co-workers [Ref. 41] clarified the conditions under which stability could be expected. Although the thermal SiO_2 provided very stable characteristics in a wet atmosphere (gaseous ambient with water vapor present) for junctions without electrical bias, or with forward bias, reverse-biased junctions were found to be affected as follows:

1. After application of reverse bias, the current increased over a period of a few hours until it reached a saturation value determined by the relative humidity, applied voltage, and oxide thickness.

2. A channel (inversion layer) was generally formed on both sides of the junction. Carrier generation in the space charge region of the channels accounted for the increase of reverse saturation current noted above.
3. The channels would be eradicated and original junction characteristics could be restored by removing the reverse bias in the presence of water vapor.

Atalla, et al., [Ref. 41] proposed that the cause of this behavior was the ability of ions on the oxide surface, made mobile by the presence of water vapor, to be sorted out in the electric field fringing the junction where it intersected the surface. Removal of the high field due to the reverse bias allowed the ions to recombine. As would be expected on the basis of such a model, the thicker the oxide over the junction, the higher the reverse bias and relative humidity required to obtain a given saturation current level.

Experimental confirmation of the Atalla model was obtained by Shockley et al. [Ref. 42], who used a Kelvin probe to measure the changes in potential of an oxide surface caused by accumulated ions on the surface. The change in surface potential, V_S , due to the motion of ions on an oxide surface of resistance R_S ohms per square, having a capacitance of C_0 farads per square meter to the underlying semiconductor, was found to obey

$$\frac{\partial V_S}{\partial t} = \frac{1}{R_S C_0} \frac{\partial^2 V_S}{\partial x^2} \quad (3.25)$$

where x is the dimension along the surface normal to the junction at $x = 0$. The solution of this equation is

$$V_S = V_0 \operatorname{erfc}(x/2\sqrt{t/R_S C_0}) \quad (3.26)$$

subject to the boundary conditions that

$$V_S = V_0 \text{ for } x \leq 0$$

$$V_S = 0 \text{ for } x > 0 \text{ at } t = 0$$

where V_0 is the potential at $x = 0$. This variation of surface potential was found to be in good agreement with the experimental results, indicating the validity of Atalia's model [Ref. 41].

In connection with this model, Schlegel et al [Ref. 43] have used a special test structure to study the drift of ions across an oxide surface due to the presence of an electric field. They point out that Equation (3.25) is derived on the assumption that the total density of ions is independent of time and distance. By allowing for the case in which the total ion density depends upon the surface potential, they obtain the equation

$$\frac{\partial V_S}{\partial t} = \frac{1}{R_S C_0} \frac{\partial^2 V}{\partial x^2} + \frac{\mu}{2} \frac{\partial^2 (V^2)}{\partial x^2} \quad (3.27)$$

where μ is the ion mobility (velocity per unit electric field) on the surface. This equation has a solution of the form

$$V = V_0 f(x^2/\mu V_0 t). \quad (3.28)$$

This solution predicts a build-up of potential (and hence surface charge) in proportion to the square root of time--as does solution (3.26) of Equation (3.25). Using (3.27) and the test structure, these authors [Ref. 43] studied surface ion motion as a function of ambient conditions. They estimated

the value for μ as 10^{-12} to 10^{-11} cm/sec per volt/cm. Ambient humidity was found to be the most important variable influencing the motion. The motion was also found to be strongly dependent upon past test history of the device.

For an exposed device immersed in a dielectric fluid which contains ions it is necessary to develop a quantitative estimate of the conditions under which surface inversion layers may be formed which will interface with proper device operation.

Consider first the electric fields present near the edge of a p-n junction where the junction intersects the surface. A reverse bias of magnitude V_a will be assumed across the p-n junction. With no ions present in the liquid surrounding the junction the electric field lines will be as sketched in Figure 3.20. The electric field lines extend from the negative charge at other surface of the p-region to the corresponding positive charges on the surface of the n-region. If the potential of the p-side is taken as zero, then the potential of the n-side is $V_0 + V_a$, where V_0 is the built-in potential across the p-n junction.

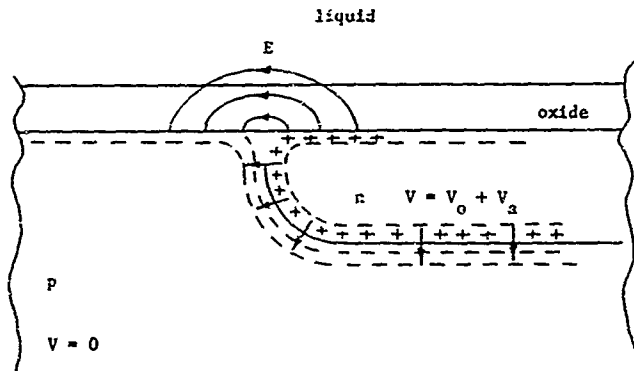


Figure 3.20. Electric field lines at reverse biased p-n junction.

The field line configuration in the dielectric region (oxide layer plus air or dielectric fluid) above the semiconductor surface near the p-n junction assuming no "free charge" in the oxide or at the oxide-dielectric fluid interface, may be determined by rigorous means through solution of Laplace's equation for the potential function $\phi(x, y)$

$$\frac{\partial^2 \phi}{\partial x^2} + \frac{\partial^2 \phi}{\partial y^2} = 0 \quad (3.29)$$

subject to the boundary conditions at the interfaces

$$\epsilon_S \frac{\partial}{\partial y} (\phi_I)_{y=0} = \epsilon_{ox} \frac{\partial}{\partial y} (\phi_{II})_{y=0} \quad (3.30)$$

$$\epsilon_{ox} \frac{\partial}{\partial y} (\phi_{II})_{y=W_{ox}} = \epsilon_f \frac{\partial}{\partial y} (\phi_{III})_{y=W_{ox}} \quad (3.31)$$

where ϵ_S = permittivity of silicon
 ϵ_{ox} = permittivity of oxide
 ϵ_f = permittivity of fluid above oxide
 W_{ox} = thickness of oxide layer

and

$$\phi = 0 \quad (3.32)$$

on the p side of the junction, and

$$\phi = V_o + V_a \quad (3.33)$$

on the n side of the junction. The solution of (3.29) subject to these boundary conditions can be lengthy. An alternate method is to use a conformal transformation to gain insight into the field line distribution.

A model for such a transformation is sketched in Figure 3.21. The coordinate system origin is taken as the midpoint of a symmetrically doped p-n junction, with the depletion region extending from $x = -a$ in the p-region to $x = +a$ in the n-region. A standard conformal transformation [Ref. 44] to the geometry shown in 3.21A allows a simple solution of Laplace's equation (3.29), which is subsequently transformed back to the original coordinate system to obtain the equipotentials and field line pattern shown in Figure 3.21B. The equipotentials appear as confocal hyperbolas and the field lines as confocal ellipses.

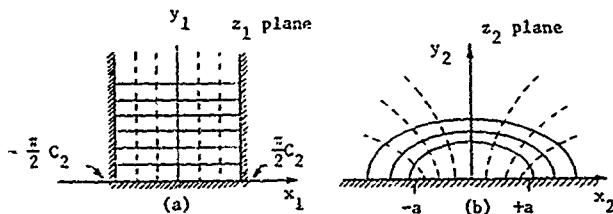


Figure 3.21. Two-angle transformation.

The magnitude of the field strength can be calculated from [Ref. 44]

$$|\vec{E}| = \left| \frac{d}{dz} \frac{V_o + V_a}{\pi} \sin^{-1}(z/a) \right|. \quad (3.34)$$

This treatment ignores the layered structure of the dielectric. Consideration of the boundary condition (3.31) indicates that the "vertical" (y) component of fields in oxide and in the dielectric fluid are related inversely as the permittivities of the two media. The tangential components of field are equal at the interface, of course. Thus, the oxide-dielectric fluid boundary refracts the field lines.

If mobile ions are present in the liquid, the negative ions will be attracted toward the n-side and positive ions will be attracted toward the p-side. This will eventually result in a positive charge layer above the n-side and a negative charge layer above the p-side as shown in Figure 3.22. This ion accumulation has the effect of decreasing the electric field in the liquid above the ion layers, and at the same time increasing the electric field inside the oxide and at the semiconductor surface. If the ion accumulation is sufficiently large and/or the oxide is sufficiently thin this increased oxide field can cause surface inversion.

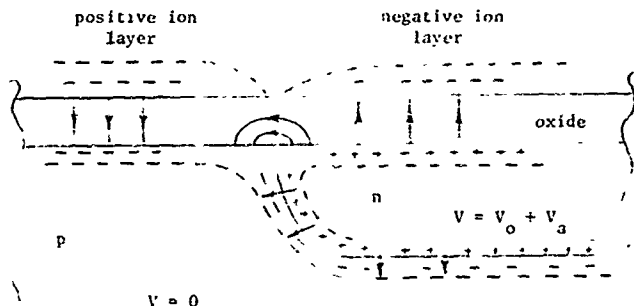


Figure 3.22. Accumulation of ions above the oxide.

The above picture has to be modified some if the liquid is in contact with a large area ground plane such as a metal housing. With the situation shown in Figure 3.22, the bulk of the liquid is at some positive potential with respect to the assumed zero of potential of the p-type region. If there is a large area ground plane present in the liquid the bulk of the

liquid will be near zero potential and the steady state ion distribution will be shown in Figure 3.23.* In this case only negative ions can accumulate above the n-type region which is at a positive potential. If the p-type region were at a negative potential and the n-type region were at zero potential, positive ions would then accumulate above the p-type region and no ions would be above the n-type region. Since these cases are symmetrical, only the case shown in Figure 3.23 need be considered.

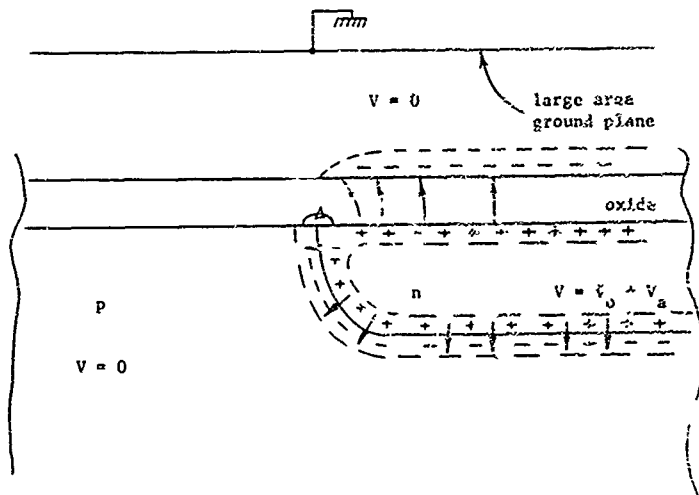


Figure 3.23. Charge distribution with large area ground plane.

In steady state the accumulated ions above the n-region will have a surface charge density exactly balancing the charge per unit area within

*The potential of the bulk of the liquid may not be exactly at zero potential but will be close to zero. The bulk potential will depend on the relative areas of the ground plane and the area of the n-type region as well as the oxide thickness. For a large area ground plane it should be very close to zero. In any case the assumption of zero potential leads to a worst case analysis of the oxide field.

the semiconductor. A steady state voltage equation can be written across the space charge layers and through the oxide which states

$$V_o + V_a = V_S + V_{ox} + V_{Si} \quad (3.35)$$

where

V_S = potential across the negative ion layer in the liquid

V_{ox} = potential across the oxide

V_{Si} = potential across the semiconductor space charge layer.

If the surface charge is not large enough to form an inversion layer, the V_{Si} term can be written as

$$V_{Si} = \frac{qN_D}{2\epsilon_S} w_d^2 \quad (3.36)$$

where

N_D = donor doping level in semiconductor

w_d = width of space charge layer in semiconductor.

If we let σ_S equal the charge per unit area in either the ion layer or the semiconductor, then:

$$qN_D w_d = \sigma_S \quad (3.37)$$

and

$$V_{Si} = \frac{\sigma_S^2}{2\epsilon_S qN_D} \quad (3.38)$$

The oxide potential is

$$V_{ox} = E_{ox} W_{ox} \quad (3.39)$$

or since

$$\epsilon_{ox} E_{ox} \approx \sigma_S \quad (3.40)$$

$$V_{ox} \approx \sigma_S \frac{W_{ox}}{\epsilon_{ox}} \quad (3.41)$$

The remaining term V_S is the potential drop across the liquid ion layer.

The ion layer will be in equilibrium between drift and diffusion effects and

$$\begin{aligned} N_S &= \text{surface ion concentration} \\ &= N_O e^{qV_S/kT} \end{aligned} \quad (3.42)$$

where

$$N_O = \text{bulk ion concentration.}$$

The ion concentration will also decay approximately exponentially with distance as

$$N = N_O e^{-x/L_D} \quad (3.43)$$

where L_D is the Debye length given by

$$L_D = \sqrt{\frac{\epsilon kT}{2q^2 N_S}} \quad (3.44)$$

where ϵ_k is the liquid dielectric constant. Then from the above

$$\sigma_S = qN_S L_D = qN_S \sqrt{\frac{\epsilon_k kT}{2qN_S}} \quad (3.45)$$

or

$$N_S = \frac{\sigma_S^2}{\epsilon_k kT} \quad (3.46)$$

The surface potential is then

$$V_S = \frac{kT}{q} \ln \frac{N_S}{N_0} = \frac{kT}{q} \ln \left(\frac{\sigma_S^2}{\epsilon_k kT N_0} \right) \quad (3.47)$$

Substitution of the expressions for the component voltages in terms of the surface charge concentration σ_S gives

$$V_0 + V_a = \frac{\sigma_S^2}{2\epsilon_S qN_D} + \tau_S \frac{W_{ox}}{\epsilon_{ox}} + \frac{kT}{q} \ln \frac{\sigma_S^2}{\epsilon_k kT N_0} \quad (3.48)$$

For a given applied voltage and other parameters, the above equation determines the surface charge σ_S (in coulomb/unit area) present in the ion layer.

The above expression is valid as long as the semiconductor contains only a depletion layer. If σ_S is sufficiently large an inversion layer will form. When this occurs the above expression from V_{S1} must be modified. When the inversion layer forms, V_{S1} remains fixed at approximately its value at the onset of inversion. If this value is indicated by V_{S1}^{-1} , then for surface inversion

$$V_0 + V_a = V_{S1}^{-1} + \sigma_S \frac{W_{ox}}{\epsilon_{ox}} + V_S \quad (3.49)$$

for $\sigma_S \geq \sigma_{Si}$, where σ_{Si} is the value of surface charge at the onset of surface inversion.

An approximate condition for avoiding surface inversion can be obtained from the above equation. The term V_{Si}^* is known if the bulk doping is known. In fact V_{Si}^* will be approximately equal to V_a . They are exactly equal if the p-n junction is symmetrically doped (i.e., $N_D \approx N_A$). In any case, they will differ at most by a few tenths of a volt.

Then to a good approximation at the onset of inversion

$$V_a = \sigma_{Si} \frac{W_{ox}}{C_{ox}} + V_S. \quad (3.50)$$

The V_S term depends on the ion concentration in the liquid. For large ion concentrations this term approaches zero. Thus if we require that there be no surface inversion when this term is neglected, surface inversion can then not occur regardless of the liquid ion concentration. Then neglecting the V_S term surface inversion will not occur provided^{1/}

$$W_{ox} \geq \frac{V_a C_{ox}}{\sigma_{Si}}. \quad (3.51)$$

The surface charge required for inversion is a well known solid state quantity and is given by

$$\sigma_{Si} = q \sqrt{\frac{\epsilon_S k T N}{q^2}} \ln\left(\frac{N}{N_i}\right), \quad (3.52)$$

^{1/} This equation assumes zero oxide charge. If the oxide has a net charge, the value of σ_{Si} in this equation should be replaced by $\sigma_{Si} + \sigma_{ss}$, where σ_{ss} is the effective surface state and oxide charge per unit area. This will either increase or decrease the required W_{ox} depending on the sign of σ_{ss} .

where N is the bulk doping in the semiconductor. Then to prevent surface inversion requires

$$\frac{W_{ox}}{V_a} \geq \frac{C_{ox}}{q \sqrt{\ln(N/N_1)}} \sqrt{\frac{q^2}{C_S k T N}} \quad (3.53)$$

This equation can be used for the oxide either an n-type region or a p-type region.

A graph of this relationship as a function of doping is shown in Figure 3.24. As an example of the magnitude involved consider $1 \text{ } \Omega \text{ cm}$ n-type silicon. This corresponds to a doping level of about $5 \times 10^{15} / \text{cm}^3$. From Figure 3.24 to prevent inversion requires that

$$\frac{W_{ox}}{V_a} \geq 0.2 \text{ } \mu/\text{volt}.$$

A $1 \text{ } \mu (10^{-4} \text{ cm})$ oxide can then sustain a voltage of 5 volts before inversion occurs.

With properly designed integrated circuits, the ions in the liquid should not cause any problems with surface inversion. The reason for this is that all properly designed integrated circuits will already be designed with oxides thick enough to prevent inversion. Because the interconnections in integrated circuits are done by metals over the oxide on the device surface, the oxides in an IC must be thick enough so that the maximum voltages applied to the metal interconnects will not cause surface inversion. This requirement on metal interconnects is the same requirement as that discussed above where the potential drop across the ion layer is negligible. Thus with properly designed IC's the oxide will

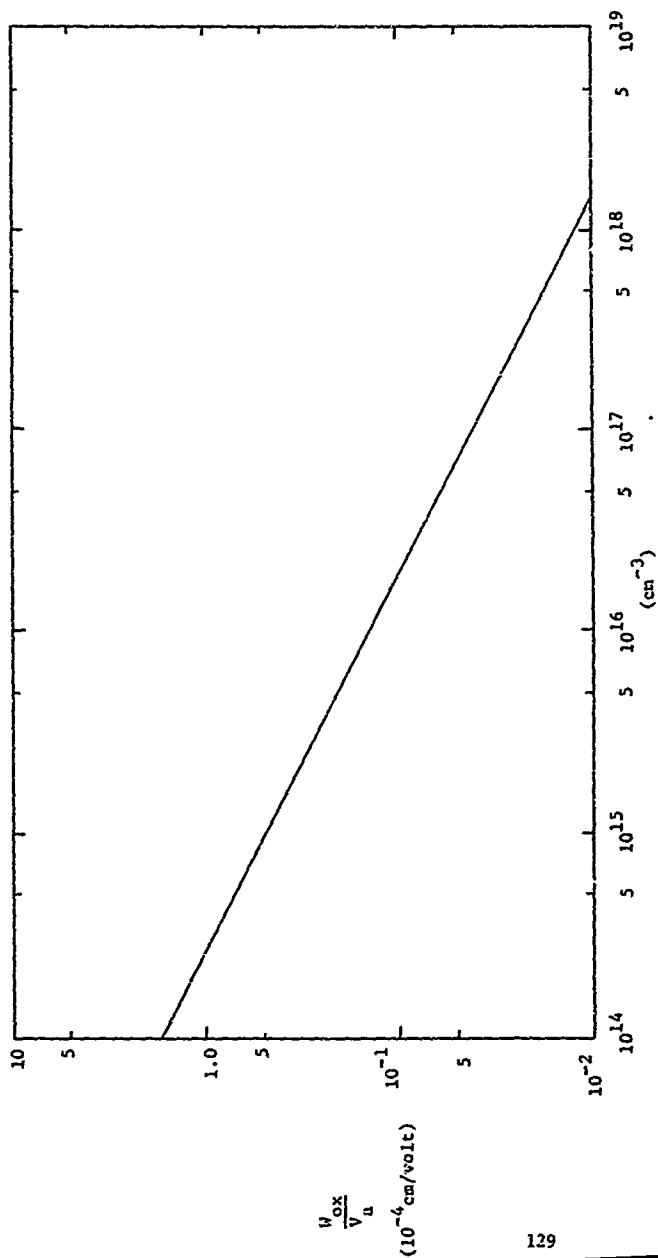


Figure 3.24. Value of W_{ox}/V_a needed to prevent inversion as a function of bulk doping.

automatically be thick enough to prevent surface inversion. This conclusion applies to both bipolar and MOS IC's. With discrete devices this requirement is not an inherent design constraint. Consequently some discrete devices might show surface inversion problems with ions from the liquid.

In addition to the motion of ions on the surface of SiO_2 layers, motion within the bulk oxide has been extensively studied. The development of stable metal-oxide semiconductor field effect transistors (MOSFETS) has been critically dependent upon methods for minimizing and preventing ionic charge motion in the oxide between the gate electrode and the semiconductor region beneath the gate. The model for this effect is shown in Figure 3.25. Positive ions, indicated by + are shown in Figure 3.25A distributed through the bulk of an oxide layer between the metal gate G and a semiconductor channel region. If the concentration of ions is sufficiently large, the surface of the semiconductor may be inverted, i.e., changed from p-type to n-type. Some order of magnitude values of charge concentrations for typical doping levels will be considered below. In Figure 3.25B a negative bias is shown applied between the gate and source electrodes which cause drift of the positive ions toward the gate in the electrostatic field. Application of a positive bias, shown in Figure 3.25C, will cause a drift of ions toward the semiconductor surface. These, plus the applied bias, create an inversion layer in the vicinity of the oxide-semiconductor interface.

The charge motion in the oxide can cause a drift of the MOSFET operating characteristics with time. Snow, Deal and their co-workers have studied the phenomena of ion drift in detail [Ref. 45]. They point out that alkali ions, particularly sodium, are the most likely contaminants involved in such drift. Concentrations on the order of 1 part per million are sufficient

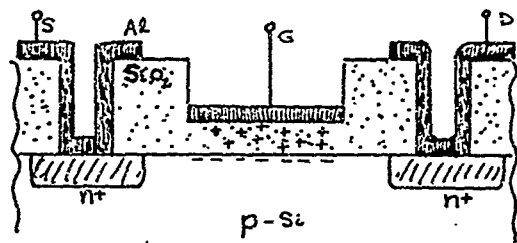


Figure 3.25 A. Initial condition. No bias applied to MOSFET. Positive ions distributed in oxide bulk.

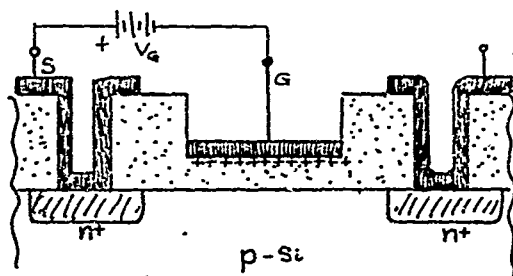


Figure 3.25 B. Negative gate-to-source bias applied. Positive ions attracted toward gate.

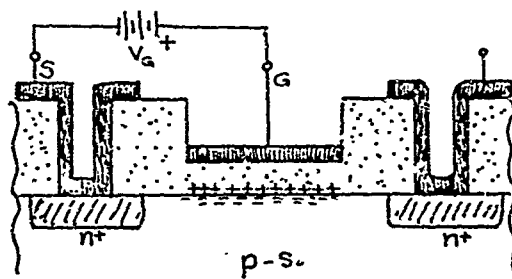


Figure 3.25 C. Positive gate-to-source bias applied. Positive ions driven by field toward semiconductor surface.

to give significant drift effects. They show that for a general distribution of charge density $\rho(x)$ per unit volume, as shown in Figure 3.26, the charge per unit area induced in the gate metal is

$$Q'_G = \int_0^x \frac{x - x_G}{x_0} \rho(x) dx \quad (3.54)$$

and the charge per unit area induced in the semiconductor at the surface is

$$Q'_S = \int_0^x \left(\frac{-x}{x_0} \right) \rho(x) dx \quad (3.55)$$

where

$$Q'_S + Q'_G = -Q_G = -\int_0^x \rho(x) dx \quad (3.56)$$

and Q_0 is the total equivalent charge per unit area in the oxide.

To obtain an idea of the order of magnitude of the effects of such an oxide charge, consider the following situation. The oxide thickness under the gate is $0.1 \mu\text{m}$ (1000 \AA). Assume that the charge is uniformly distributed in the oxide, i.e., $\rho(x) = \rho_0$, a constant. Then, from (3.54) and (3.55)

$$Q'_G = \rho_0 \int_0^{x_0} \left(\frac{x - x_G}{x_0} \right) dx = -\rho_0 x_0 / 2$$

$$Q'_S = -\frac{\rho_0}{x_0} \int_0^{x_0} x dx = -\rho_0 x_0 / 2$$

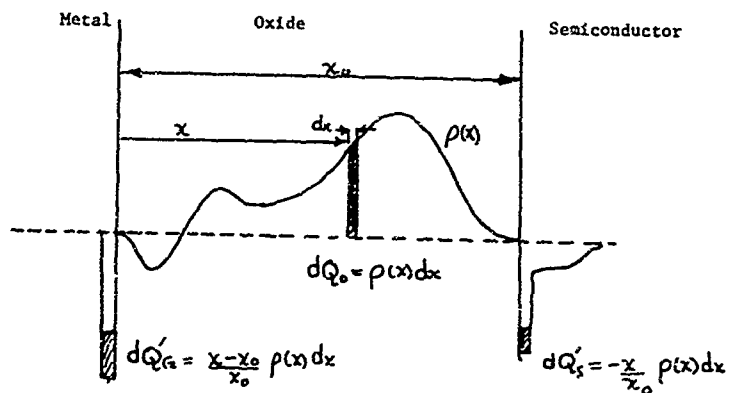


Figure 3.26: Increments of charge induced in gate metal and in semiconductor due to an increment of distributed charge in the oxide bulk [Ref. 45]

and $Q_0 = -\rho_0 x_0$ from equation (3.56). For an acceptor doping level of 2×10^{16} per cm^3 of the semiconductor, an induced semiconductor surface charge of about 4×10^{11} e per cm^2 (where e is the magnitude of the charge of one electron) will be sufficient to make the surface intrinsic. This can be induced by an oxide charge of

$$\rho_0 = 2e \times 4 \times 10^{11} / 10^{-5} = 8 \times 10^{16} \text{ e per cm}^3.$$

The effect of the distributed charge is equivalent to a voltage impressed on the gate of about

$$\Delta V = -\gamma'_S / C_0 \quad (3.57)$$

where C_0 is the capacitance per unit area of the MOS structure. Since the dielectric constant of SiO_2 is about 4.0, the C_0 value for the assumed oxide thickness of 1000 Å is

$$C_0 = 4.0 \times 8.85 \times 10^{-14} / 10^{-5} = 3.54 \times 10^{-8} \text{ f/cm}^2.$$

The equivalent voltage from equation (3.57) is

$$\Delta V = - \left(\frac{4 \times 10^{11} \times 1.6 \times 10^{-19}}{3.54 \times 10^{-8}} \right) = 1.8 \text{ volts}.$$

This increment of potential acts in addition to any potential which is applied to the gate by an external bias source. If the oxide charge has drifted to the metal-oxide interface, the equivalent voltage shift is zero since a matching charge is induced in the metal. On the other hand, drifting

of the oxide ions to the vicinity of the semiconductor interface can cause an equivalent voltage shift of about

$$\Delta V = 3.6 \text{ volts.}$$

Therefore, the drifting back and forth of ions can cause shifts ranging from 0 to almost 4.0 volts in the gate to source voltage characteristic.

In addition to sodium ions, it has been shown [Ref. 46] that protons in the oxide can be drifted under the influence of an electric field. Contaminating protons can be obtained from adsorbed organic vapors or water vapor or from the reaction of aluminum (frequently used for gate metallization) and water vapor [Ref. 47]. Hofstein [Ref. 46] gives a diffusion coefficient of

$$D = \exp(-0.73/kT) \text{ cm}^2/\text{sec} \quad (3.58)$$

for protons in SiO_2 in a field of 2×10^5 volts/cm. At 100°C this has the value of about $6 \times 10^{-6} \text{ cm}^2/\text{sec}$. In contrast, the diffusion constant for sodium in SiO_2 at 100°C is about $3 \times 10^{-12} \text{ cm}^2/\text{sec}$ (using data from McDonald [Ref. 48]). Thus, the motion of protons through SiO_2 is much more rapid than that of sodium ions.

Many of the experiments performed on sodium and proton contamination of oxides have used high concentration sources of these ions deliberately placed on the surface and then diffused into the oxide at relatively high temperatures, typically 250 to 300°C [Ref. 46], or 200°C [Ref. 45]. Using the results of Snow et al [Ref. 45] and McDonald [Ref. 48], the diffusion constant for sodium in SiO_2 is

$$D = 10^{11} \exp(-1.39/kT) \quad (3.59)$$

and that for protons has been given above in equation (3.12). Regarding the source at the surface as constant, the concentration at a distance x into the oxide is given by [Ref. 49]

$$c(x) = c(o) \operatorname{erfc}(x/2\sqrt{Dt}) \quad (3.60)$$

The extent of diffusion from a surface source will depend upon the contaminant concentration at the surface $c(o)$, the temperature--through its effect on D --and the time, t , over which the diffusion has occurred.

Several different materials have been tried as barriers to ionic (particularly sodium) transport in SiO_2 . Among the glassy layers, phosphosilicate glass (PSG) [Ref. 50] has been effective as a barrier and as a "getter" to immobilize sodium ions but is subject to polarization effects which may affect device stability. A more satisfactory material is silicon nitride (Si_3N_4). Layers of Si_3N_4 thicker than 200 Å are effective in inhibiting proton motion [Ref. 47]. A layer 1000 Å thick (0.1 μm) over SiO_2 has been found to reduce the amount of sodium reaching the SiO_2 -Si interface by a factor of 1000 [Ref. 51]. Application of this protection has been effective in preventing degradation of current gain in bipolar transistor structures [Ref. 48] and has been applied to high volume production of npn transistors by the Western Electric Company [Ref. 52]. For several years nitride passivated integrated circuits have been produced and used by the Bell system and others.

Although nitride passivation has proved effective in preventing device instability due to ionic drift in the passivation layer over the device, it cannot cure the problem of drift due to the accumulation of a charge layer on the surface of the device. In bipolar devices [Ref. 48], an accumulation

of surface charge on the order of 5×10^{11} per cm^2 can drastically reduce the current gain, at low collector current levels, of npn transistors. Much higher concentrations (about 9×10^{12} per cm^2) are required to degrade pnp current gain due to inversion of the emitter region surface. When considering performance degradation due to increased leakage current in the collector base junction, however, pnp transistors are much more susceptible than npn transistors to surface ionic accumulations. This is particularly true when the induced channel region spreads to where surface defects can be encountered. At these defects there is a much higher carrier generation-recombination rate, leading to a rapid increase in leakage current [Ref. 53]. The standard method for preventing this is to diffuse a ring of highly doped material around the periphery of the chip to prevent the channel from extending to the highly disturbed scribe lines at the edge of the chip [Refs. 52, 53]. Another method is to use an additional metal ring ("Equipotential ring") to overlap the junction region to prevent inversion layers from forming [Ref. 48].

In addition to electrostatic effects, electrochemical effects occur on semiconductor surfaces, which may result in device degradation and eventual failure [Ref. 54]. Aluminum, widely used for metallization of transistors and integrated circuits, will react with water in the presence of trace quantities of ions of chlorine, ammonium, copper and iron, among others. The reaction will continue as long as water is available and may eventually lead to an open circuit. Built-in potential differences due to couples of dissimilar metals or p-n junctions can locally enhance this corrosion. Gold, another commonly used conductor, is susceptible to gradual dissolution by water when chloride ions are present.

Protection against such corrosion can be obtained by coating the device with a polymeric moisture barrier. Silicone resins have been found effective for this purpose [Ref. 55]. Another method is to use a glass frit suspended in a volatile liquid. Application of heat at a few hundred degrees centigrade evaporates the liquid and fuses the frit to form a glass envelope over the circuit. If the glass layer is too thick, thermal stresses promote cracking. One investigation has reported that 2 to 2.5 micrometers will provide satisfactory protection without cracking [Ref. 56]. These coverings, along with the increasing use of Si_3N_4 passivation signal efforts by the semiconductor industry to provide hermeticity at the chip level, in order to obviate the need for hermetically sealed packages. These are expensive and the industry would prefer to replace them with plastic encapsulation wherever possible.

In summary, past experience with ionic contamination of semiconductor devices has shown that such contamination can significantly affect the operation of these devices by changing parameters such as leakage currents, transistor current gain and p-n junction breakdown voltages or by corroding metallization. In recent years there has been an increasing effort by the semiconductor industry--urged and financed in large measure by DOD--to provide more effective protection against such contamination at the chip level. At present, however, few devices are available with such protection. Consequently, it is highly probable that most semiconductor devices used by a system design engineer for outboarded electronic systems for the next few years at least will still be susceptible to ionic contamination of the chip. If subsequent analysis and test programs indicate that there will be ionic contaminants present, there will be a need to identify a suitable passivating material which could be routinely applied to chips ear-marked

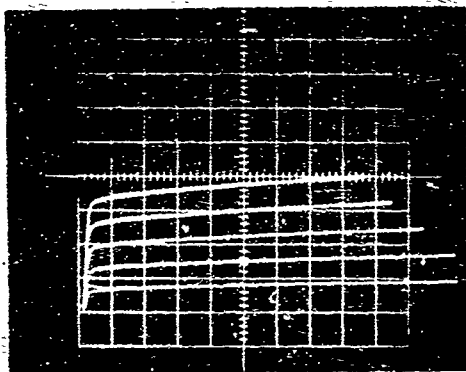
for immersed system operation. At present the most likely candidate is a conformal polymeric coating, applied and cured at temperatures too low to degrade the properties of the semiconductor device.

3.3.2 Experimental

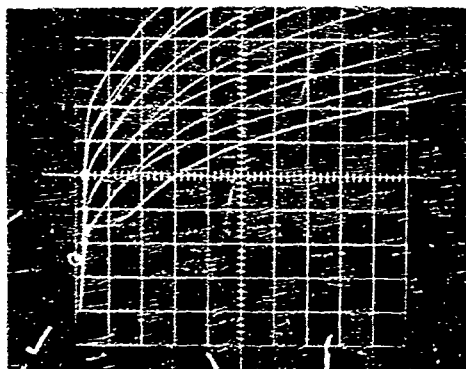
When opening TO-cans containing germanium alloy transistors, either high power types or small signal types, it was noted that exposure to laboratory atmosphere caused an immediate shift of collector I-V characteristic curves. Generally leakage current was increased and the slope of the curves increased. This is illustrated in Figure 3.27 which shows the change in characteristic curves for a 2N1412 (Ge alloy, PNP, 150 watt rating, manufactured by Motorola). Immersion in EC 200^{*} in the pressure chamber restored the original curve shapes to a large extent initially, as shown in Figure 3.28. Also shown in Figure 3.28 are the consequent shifts when the device was pressured to 3000 and to 6000 psi. The last change was abrupt and the curves remained with this shape when the pressure was reduced to one atmosphere. The device was apparently mechanically damaged, evidenced by sensitivity to probing around the periphery of the base.

Small signal Ge alloy transistors, type 2N526, were also found to change characteristics when exposed to laboratory atmosphere or immersed in DC 200 for a short time. In one case, a coating of room temperature vulcanizing silicone rubber, KTV 3144^{*} was used to coat a 2N526 transistor chip immediately after the cap was removed. This was cured overnight at room temperature. The transistor was tested to 14000 psi and found to keep the original collector I-V curve shape. This confirmed the theoretical prediction that pressure, per se, up to 1000 atmospheres would not significantly influence device operation. It also indicated that an effective passivant would allow operation to deepest ocean pressures.

^{*} Dow Corning product.

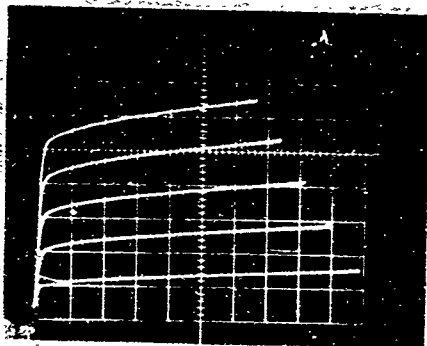


A. Collector I-V curves at room temperature prior to opening of package (T0-36)

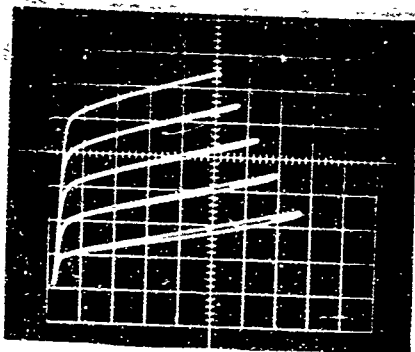


B. Collector I-V characteristics at room temperature after package has been opened and device exposed to laboratory atmosphere.

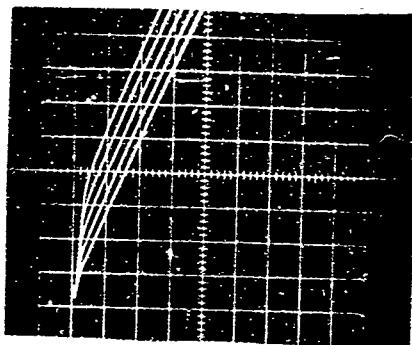
Figure 3.27: Collector I-V curves for 2N1412 PNP Ge alloy power transistor



A. In DC 200 in pressure chamber at 1 atmosphere



B. At 3000 psi.



C. At 1 atmosphere after pressuring to 6000 psi where curves abruptly changed to shape shown at left.

Figure 3.28: Ge Alloy Transistor (2N1412) in silicone oil under various pressures.

Silicon transistors, both power and small signal, bipolar and MOSFET showed no significant change in operating characteristics when exposed to laboratory atmosphere or DC 200. Even when an attempt was made to contaminate DC 200 with aqueous NaCl solution--of the same chloride ion concentration as sea water--no changes were noted. It should be pointed out that these were short term tests, several days at most.

Very dilute solutions of NaCl, 150 ppm salt concentration, in distilled, demineralized water were applied directly to the silicon chips of small signal, 1~ noise transistors, Fairchild types 2N2483 and 2484. Typically, the base-emitter forward bias curves were recorded before the hermetic seal was broken, immediately after opening in laboratory atmosphere. after the dilute salt solution was applied and dried in room temperature air, and after the salt residue was thoroughly rinsed away by distilled, demineralized water (ddH_2O) and the unit dried in air or nitrogen.

Figure 3.29 shows the result of one series of tests. The low level emitter-base current is increased by a factor of about 200 by exposure to laboratory air. Not much improvement was gained in a humidifier. Another 200 fold increase is obtained due to the salt solution residue on the device. That this is a surface effect is evidenced by the restoration of "original" in air behavior following a ddH_2O rinse and drying in nitrogen.

An effort to repeat the process on the same unit was not successful because of an open circuit which developed when the Al lead wire from one of the posts in the header to the emitter metallization parted near the post. Although this might be attributed to mechanical failure due to rinse water impinging on the wire, it was probably enhanced by chlorine corrosion of the aluminum. Evidence for this was secured with two other

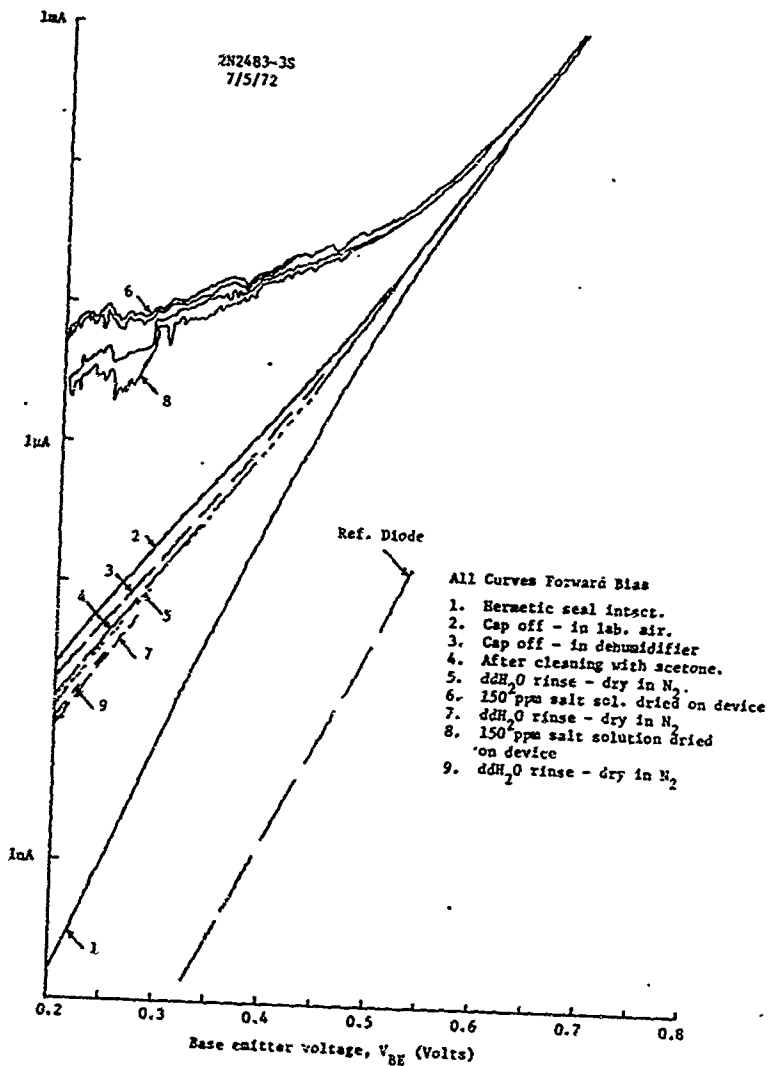


Figure 3.29

2N2483 devices which were deliberately contaminated with "as is" seawater followed by an acetone rinse or a ddH₂O rinse. In both cases, a lead opened up. In one of these devices, the progress of the deterioration could be followed. Curves for this device, 2N2483-25, are shown in Figure 3.30. It had previously been contaminated with 150 ppm salt solution and rinsed in acetone, to avoid complete removal of the salt. The series of curves was taken with electrical bias applied only during the time taken to plot the curve, about 30 seconds. The aluminum wire base lead had parted and the aluminum metallization appeared to be severely attacked.

Although the use of undiluted seawater is unrealistic from the point of view of oil immersed operation, the rapidity of the failure points out the problem that may result from long term exposure to much lower levels of contaminants. First, there can be an electrical effect on device parameters, particularly in low level signal processing, and secondly, there can be corrosive attack on the devices if the oil becomes contaminated.

A long term immersion test was initiated using some devices which had been previously opened and pressure tested as well as some which had not. Eight MOSFET devices, tabulated below in Table 3.5, were decapped and immersed on 4/10/72 in Dow Corning 200 silicone oil. No attempt was made to contaminate the oil other than the natural contamination due to routine handling of the components and circuit boards. Prior to immersion, photographs were made of the characteristic curves for each device and the drain to source voltage drop was measured for each device in thermal equilibrium in laboratory air with a supply voltage of 10 volts. Following immersion, the supply voltage was increased to 15 volts to bring device dissipation close to the rated 250 milliwatt value during the immersion.

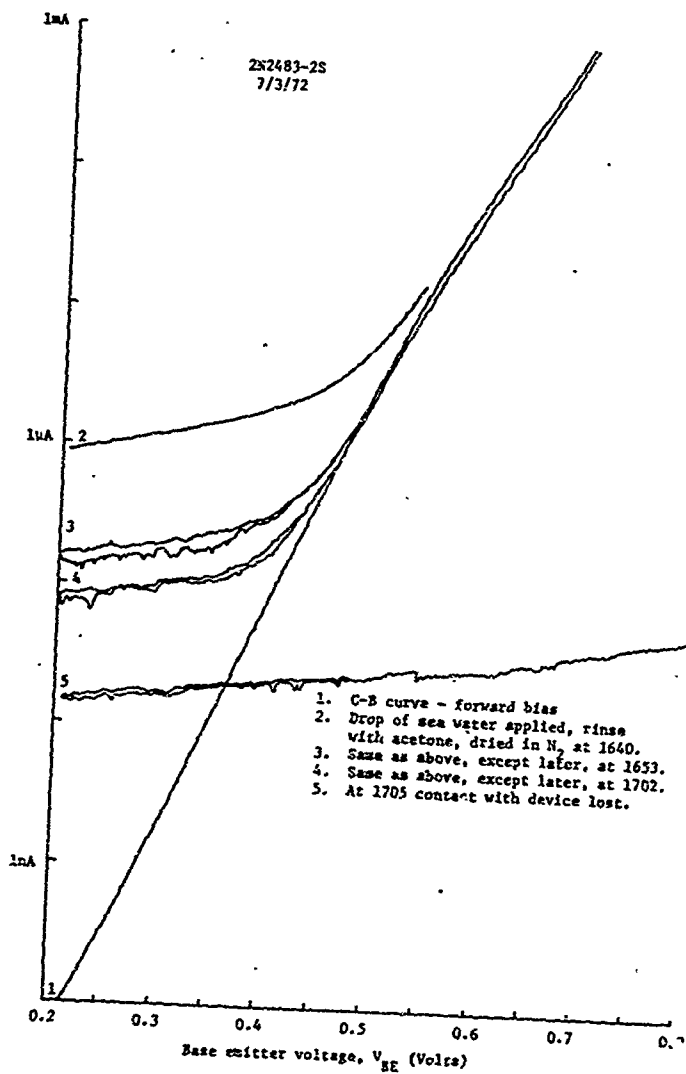


Figure 3.30

Table 2.5: Percentage change in MOSFET drain currents on various days, compared to initial drain current

Device	Percentage change in drain current on date				
	9/29/72	11/6/72	11/6/72*	11/7/72	3/12/73
3N157-13	+14	+14	+14	+21	+14
3N157-12	+50	+67	+67	+75	+67
M163-2	+20	+20	+20	+20	+20
M163-1	+6	+6	+6	+12	+6
3N152-2	+2	+2	+2	+23	+20
3N152-1	+9	-3.5	-3.5	-3.5	-4.0
2N3796-4	+4.7	+250	+13	+10	0
2N3796-3	0	-2.5	-2.5	-5	-7.5

*Following TCE and acetone cleaning

Bipolar devices were checked in a similar manner prior to immersion.

Figures 3.31 and 3.32 show the circuit diagrams used for both bipolar and MOSFET devices. Oil bath temperatures were about 40°C.

During 11 months of immersion, the exposed bipolar devices showed a drift of collector current of only 5.5 percent maximum. This was not uniform, but has varied from time to time. This variation was within that expected from meter accuracy and changes in ambient temperature of a few degrees centigrade. Immersed operation appears not to have changed these devices.

For the MOSFET devices, there was an initial shift in current values from the time of first immersion to the check made about six months later. The amount of this shift and that measured for each of the devices on subsequent measurements is shown in Table 3.5. Except for one device, the amount of device current change, referred to the initial value, appeared to be relatively stable. On 11/6/72, approximately 7 months after the

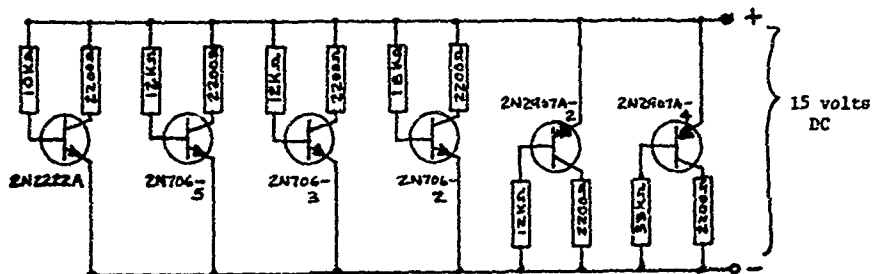


Figure 3.31: Bias circuit for bipolar transistors in long term immersion in silicone oil

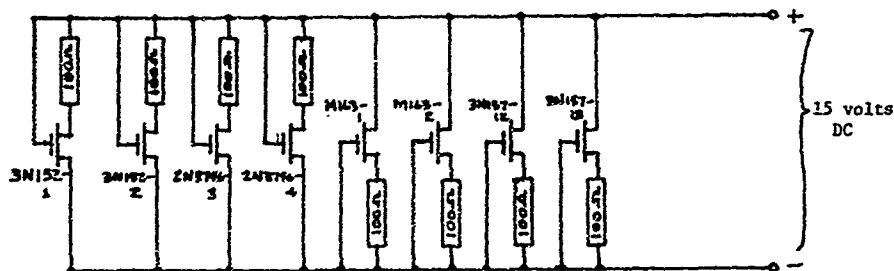


Figure 3.32: Bias circuit for MOS field effect transistors in long term immersion in silicone oil

initial immersion, the radical increase in the current of device 2N3796-4 prompted a closer look at the test devices.

Since it is well known that the capacitance of the MOS gate-oxide-silicon structure of a MOSFET depends upon the ionic charge distribution in the oxide, among other things, provisions were made to measure this parameter for the test devices. Plots of the gate-substrate capacitance as a function of voltage were made for each device prior to and subsequent to surface cleaning with electronic grade trichloroethylene (TCE) and acetone. Only one device, 2N3796-4, showed an immediate effect in drain current change following the cleaning, but there was no detectable change in the C-V characteristic of this device. This indicated that no change in charge distribution in the oxide bulk had occurred, but that perhaps some surface effect was operative.

The data of Table 3.5 show that for most devices there was an increase of drain current. One possible explanation for this would be a long term drift of positive charge in the oxide. In the case of n channel devices a positive gate-source bias drifts positive charge toward the p-type silicon substrate, attracting negative charge carriers to increase the n-channel, causing more current flow. In the case of p-channel devices, the negative gate-source bias would drift positive ions toward the gate where they could be compensated by negative charge on the gate. This would remove the inhibitory effect these positive charges have on the formation and increase of a p-channel. These positive charges are "built in" during the device manufacturing process to an extent depending upon the expertise of the manufacturer in growing "clean" oxides. The drifts observed may be inherent in the as manufactured devices.

As a check, three de-capped devices and four devices with caps intact were tested. All were p-channel MOSFET's, type 3N157. These were connected as shown in Figure 3.32 except for the gate connection, which could be changed to allow connection to -15V, ground or to a pulse source for a check of pulse gain. Table 3.6 shows the change in drain-to-source voltage which occurred under various bias conditions. All voltage checks were made in air, allowing 15 minutes for temperature stabilization. After the initial check, on 10/18/72, the devices were operated in DC 200, 10 centistokes. The bias was changed as noted in the table.

In the first 24 hours following immersion, there was a decrease in current through all devices to a value which remained constant over the next four days. A twenty four hour application of a positive 15 volt gate bias followed by application of -15 volts just prior to measurement gave a further decrease in current (i.e., lower IR drops in load resistors, hence higher drain to source voltages). This effect was reversible by application of negative 15 volt bias again for a period of time. Handling of the devices took its toll. The lack of recovery shown by uncapped device 3N157-15 was followed by eventual total failure (open circuit). Similar failures of two capped devices, -20 and -21 occurred during subsequent testing such as pulse gain, CV plots, etc. Device 3N157-15 failed due to a break in the drain lead wire adjacent to the wedge bond on the drain pad of the device. The break appeared to be due to mechanical reasons. After failure 3N157-20 was also decapped and found to have a parted lead to the source. Again, this occurred at the wedge bond and appeared to be due to mechanical reasons. Device 3N157-21 was also decapped after failure. The reason for failure was a burnout of the aluminum metallization

Table 3.6: Drain to source voltage magnitude for 3N157 transistors operated immersed in DC 200, 10 c.s., under various bias conditions

Device	Condition	Drain to source voltage on date							Drain Current Percent Change
		Initial 10/18/72	10/19/72	10/23/72	10/24/72	10/25/72	10/30/72	3/12/73	
3N157-15	no cap	12.0	12.2	12.2	13.6	14.1	14.0	--	--
3N157-18	no cap	11.8	12.0	12.0	12.5	11.7	11.8	12.0	- 6.2
3N157-19	no cap	12.8	13.1	13.0	13.5	12.7	14.1	12.4	+ 18
3N157-20	cap	12.5	12.9	12.8	13.0	12.5	12.4	--	--
3N157-21	cap	12.5	12.9	12.8	13.0	12.4	14.25	--	--
3N157-22	cap	12.2	12.6	12.5	12.7	12.1	12.2	12.5	- 10.7
3N157-23	cap	12.2	12.6	12.5	12.7	12.1	12.2	12.5	- 10.7
			Note 1	Note 1	Note 2	Note 3	Note 4	Note 5	

Note 1. Gate connected to -15 volt terminal.

Note 2. Gate connected to +15 volts for 24 hours.

Note 3. Gate connected to -15 volt terminal overnight.

Note 4. Gate connected to +15 volts for 20 hours and then to -15 volts for 1.5 hours prior to check.

Note 5. Socket on 3N157-19 found defective. Replaced in circuit board.

between the source pad and the curvilinear aluminum source strip around the periphery of the device. This was due most likely to an improper insertion in an electrical circuit during testing.

As shown in Table 3.6 each device, capped or de-capped, experienced a decrease in drain current for a given bias (-15 volts) over a period of time except for 3N157-19 which experienced an 18 percent increase. This seems to contradict the results cited previously, where practically every uncapped MOSFET experienced an increase in drain current. However, in the previous test device dissipation was limited by using a 10V drain bias for measurement in air, whereas in the present test 15V was used. During the 15 minute wait for stabilization, the devices heated well above ambient. In a field effect device, the transconductance is directly proportional to the mobility of the channel charge carriers. The mobility, in turn, is a function of temperature. For the relatively lightly doped material commonly used, the mobility will vary approximately as $T^{-2.5}$ [Ref. 21]. The much higher dissipation of the second test series (about 450 m watt per device versus about 250 m watt before) would account for this shift.

Based upon the data reported above, however, the following conclusions can be drawn:

1. Bipolar devices are relatively unaffected by operation in DC 300.
2. There is some inherent drift in MOSFET transconductance characteristics under high bias (gate voltage near that of drain voltage).
3. In addition to the inherent drift, surface conditions may influence MOSFET performance.

3.3.3 Thermal Effects on Device Operation Near Transfer

As is well known, variations of temperature can cause variations in the operating parameters of semiconductor devices. Leakage current, I_L , transistor current gain, h_{FE} and junction forward voltage drop at constant current, V_{BE} , are all sensitive to temperature changes. For silicon transistors typical figures are [Ref. 57]

I_S doubles with a 12° to 15° C increase,

V_{BE} decreases at about 2 millivolts per 1° C increase.

The change in current gain with temperature depends upon the way in which the device is made. A recent study [Ref. 58] found that for an 80° C change, from -55° C to 25° C, the d-c common-emitter current gain changed as shown in Table 3.7.

Table 3.7: Change of current gain with temperature [Ref. 58]

Device Type	-55° C	25° C	$h_{FE}(25^\circ\text{C})/h_{FE}(-55^\circ\text{C})$
Single diffused	88.5	99.0	1.12
Single diffused	50.0	66.7	1.34
Mesa	46.5	79.5	1.71
Mesa	37.0	70.0	1.89
Mesa	28.0	59.0	2.10
Mesa	34.5	76.5	2.20
Planar	11.0	24.5	2.33
Planar	8.5	22.0	2.60
Planar	44.0	130.0	2.96
Planar	25.0	76.5	3.04

Many techniques have been devised by circuit designers to minimize the effects of temperature changes on circuits using semiconductor devices. Large area heat sinks are employed to improve dissipation from power controlling devices such as rectifiers, SCR's and power transistors. It is of interest to the system design engineer to know to what extent the heat transfer from semiconductor devices will be altered by immersed operation.

As is well known, many large power transformers operating at atmospheric pressure are immersed in a dielectric liquid (oil) which, among other uses, serves as a heat transfer medium. The heat transfer is usually accomplished by free convection and by conduction through the oil. Generally the heat transfer rate is significantly greater in a liquid than in air for a given temperature drop between the heated object and the surrounding medium. This fact has prompted a careful look at liquid cooling of high density microelectronic circuits. A recent study [Ref. 59] has compared free convective cooling in air with free and forced convective cooling in Freon 113 fluid and Dow Corning 209 silicone oil of microelectronic circuit chips. Figure 3.32 shows the heat flux in watts/cm² from the semiconductor surface as a function of the temperature drop from the surface, at T_s , to the ambient fluid at T_a ° C. For example, at $\Delta T = T_s - T_a = 10^\circ \text{C}$, free convective cooling by silicone oil dissipates three times as much heat per unit area as occurs in free air.

Although enhanced cooling can be expected due to immersion in the oil, consideration must be given to how the free convective heat transfer in oil might be influenced by pressure. Pressure will be expected to increase density and viscosity—leading to a decrease in convective heat

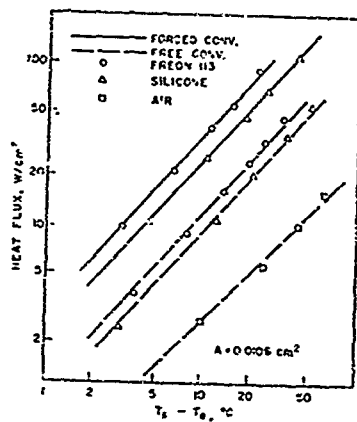


Figure 3.33: Heat flux from semiconductor surface versus temperature difference in air, Freon and silicone oil [Ref. 59]

transfer--and increase the thermal conductivity--leading to an increase in conductive heat transfer. The change in overall heat transfer rate on going from atmospheric pressure to pressures as high as 1000 atmospheres will depend upon the relative magnitudes of the opposing effects. For free convection, the heat transfer coefficient, h_c , defined by

$$h_c = q/A\Delta T \quad (3.61)$$

where q is the energy transferred per second, A the area of the dissipating surface and ΔT the temperature drop from surface to ambient fluid, is proportional to the density, ρ , viscosity, μ , and thermal conductivity, k , of the fluid as shown below [Ref. 50].

$$h_c = \text{const} \times k [L^3 \rho^2 g \beta (\Delta T) / \mu^2]^a (C_p \mu / k)^b \quad (3.62)$$

The exponents a and b depend upon the geometry of the heat dissipating surface. For horizontal square plates, the exponents are equal, $a = b$, and their value depends upon the range of values of the parameters. The dimensionless parameter group in square brackets raised to the a^{th} power in equation (3.62) is called the Grashof number, symbolized Gr , and the dimensionless parameter group raised to the b^{th} power in (3.62) is called the Prandtl number, symbolized Pr . Using parameter values typical of 10 centistoke EC200, namely

$$\rho = 0.934 \text{ gr/cm}^3$$

$$\gamma = \mu/\rho = 0.1 \text{ stoke}$$

$$C_p = 0.35 \text{ cal/gm/}^\circ\text{C}$$

$$k = 3.2 \times 10^{-4} \text{ gr cal/sec/cm}^2/^\circ\text{C/cm}$$

$$\beta = 1.08 \times 10^{-3}/^\circ\text{C}$$

[Source: Dow Corning Bulletin 22-069, dated 10/71] and assuming $L = 10$ cm.

$\Delta T = 25^\circ\text{C}$,

$$\text{Gr} = 2.65 \times 10^6$$

$$\text{Pr} = 1.02 \times 10^2$$

and the product is

$$\text{Gr Pr} = 2.71 \times 10^8.$$

According to McAdams, in this range of parameter values, $a = b = 1/3$.

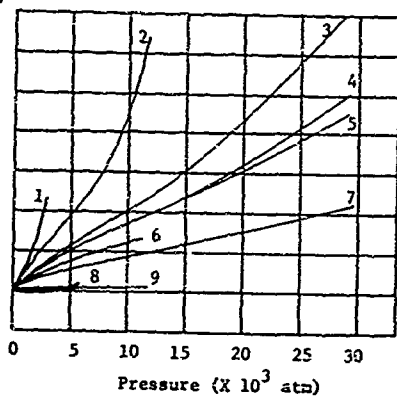
Therefore,

$$h_c \propto k^{0.67} \nu^{-0.33}$$

and the ratio of h_c at 1000 atmospheres to that at 1 atmosphere will be

$$\frac{h_c(1000)}{h_c(1)} = \left(\frac{k}{k_o}\right)^{0.67} \left(\frac{\nu_o}{\nu}\right)^{0.33} \quad (3.63)$$

where the o subscripts denote reference (1 atmosphere) conditions. The variation for fluids of thermal conductivity and viscosity with pressure depends upon the complexity of the molecules of the fluid. Viscosity varies roughly exponentially with pressure, as shown in Figur. 3.34A [Ref. 29, p. 82]. Thermal conductivity, however, increases a lower rate with increasing pressure. Data on two different fluids, methyl alcohol and iso-amyl alcohol [Ref. 29, p. 92] is plotted in Figure 3.34B. The variation is slightly sublinear. For the two fluids shown, even though of different molecular structure, the increase is about the same--roughly 20 percent at



1. Eugenol (30°C)
2. Silicone $(\text{CH}_3)_3\text{SiOSi}(\text{CH}_3)_2\text{OSi}(\text{CH}_3)_3$
3. $i\text{-C}_3\text{H}_7\text{OH}$
4. $i\text{-C}_5\text{H}_{12}$
5. $n\text{-C}_3\text{H}_7\text{OH}$
6. $\text{C}_2\text{H}_5\text{OH}(30^\circ\text{C})$
7. CH_3OH
8. $\text{H}_2\text{O}(0^\circ\text{C})$
9. $\text{Hg}(30^\circ\text{C})$

Figure 3.34A: The viscosities of some compressed liquids. The measurements were made at room temperature unless it is otherwise indicated [Ref. 29].

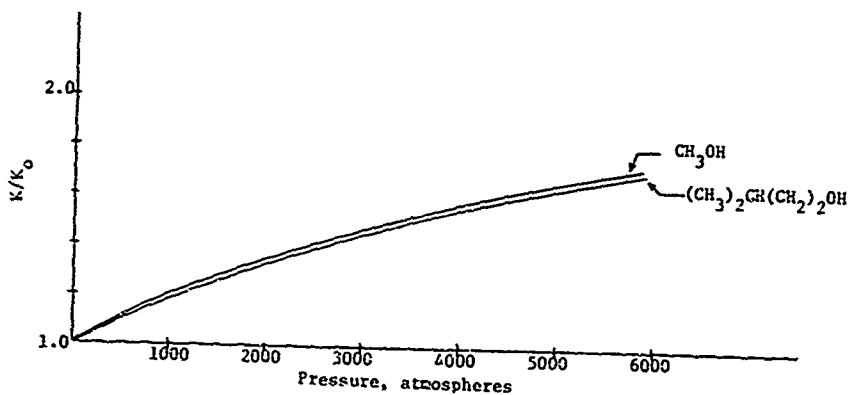


Figure 3.34B: Change of thermal conductivity with pressure for a liquid of simple molecular structure and a liquid of complex structure [Ref. 29].

1000 atmospheres and 33 percent at 2000 atmospheres. Using the curve for silicone fluid in Figure 3.34A, there is about a threefold increase of viscosity at 1000 atmospheres. Using a 20 percent increase in thermal conductivity at 1000 atmospheres as typical,

$$\frac{h_c(1000)}{h_c(1)} = (1.2)^{0.67} (0.33)^{0.33} = 0.79 .$$

There will be about 21 percent reduction in heat transfer capability due to the pressure.

As a test of whether or not this optimistic forecast can actually be achieved, two power transistors in TO-66 cans were de-capped to allow operation in contact with DC 200 silicone oil, 10 centistokes viscosity, at pressures ranging from atmospheric to 15,000 psi. The silicon chips of both devices were coated with a white polymeric substance by the manufacturer, Motorola. The planar silicon power transistors, a 2N4232 (NPN) and a 2N3740 (PNP) were connected as shown schematically in Figure 3.35. The circuit board was attached to the sheathed iron constantan thermocouple which penetrates the pressure chamber along with the electrical leads. The position is shown in Figure 3.36. The voltage drops V_1 , V_2 , V_3 and V_4 indicated on Figure 3.35 were monitored to determine base and collector currents in the devices. These were monitored with the devices operating at DC 200 at atmospheric pressure, 5000 psi, 10000 psi and 15000 psi.

A plot of the power dissipated by each transistor and the collector current of each as a function of time is given in Figure 3.37. Also shown is the oil temperature indicated by the monitoring thermocouple. Each time the chamber pressure was increased the temperature increased for a short time and then settled back. The collector currents and power

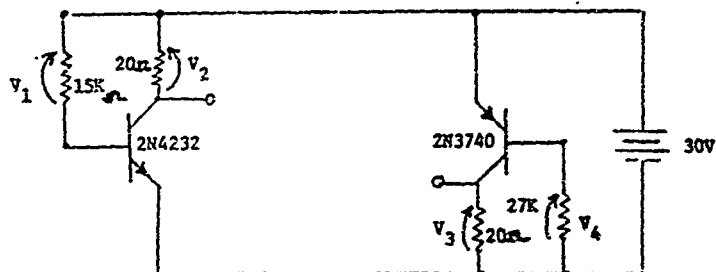


Figure 3.35: Schematic diagram of power transistor bias circuits for heat transfer tests.



Figure 3.36: Test arrangement of silicon power transistors for heat dissipation test.

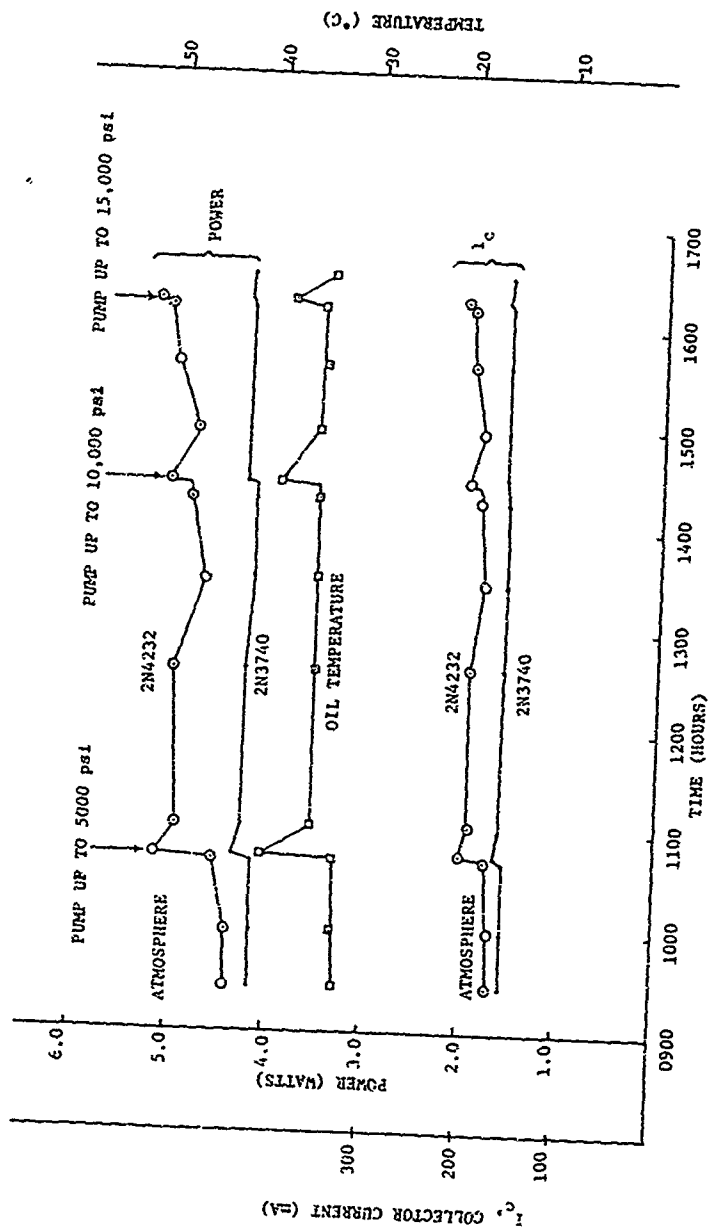


Figure 3.37: Power transistor dissipation rates and collector currents and oil temperature versus time during heat transfer tests.

dissipation of the transistors followed these temperature variations, with the NPN 2N4232 apparently more sensitive to the changes than the PNP 2N3740.

Although the temperature indicated by the thermocouple remained relatively constant—except for pump up surges—the transistor currents fluctuated somewhat, with the fluctuations of the 2N232 larger than those of the 2N3740. The input base currents during the experiment varied by less than one percent in the case of the 2N4232 and about two percent in the case of the 2N3740. These variations did not always synchronize with the collector current fluctuations. A possible reason for the 2N4232 device fluctuations appeared when this device failed—at 12000 psi after having been pressured to 15000 psi. Subsequent examination revealed that the emitter lead had parted from the terminal post. The stitch bond on this lead had been made at the very edge of the post. The leads to the metallization on the chip are protected by a polymeric coating against vibrational stresses, but not at the post. It is likely that the vibration created during removal of the top of the cap ruptured the bond, but it did not part until late in the experiment, for an unknown reason. It is possible that adhesion between the polymeric coating and the lead was good enough to support forces leading to rupture of a previously weakened bond. A schematic sketch of this is shown in Figure 3.38. The bulk modulus of polymeric materials is generally much lower than that of many other solids, leading to greater deformation under pressure. Such deformation is suggested by the arrows in the polymeric coating in the sketch. The total force developed along the wire, symbolized by the reaction force F_B developed at the bond area, may be sufficient to rupture the bond, particularly if it has been previously weakened by vibration or other mechanical stress.

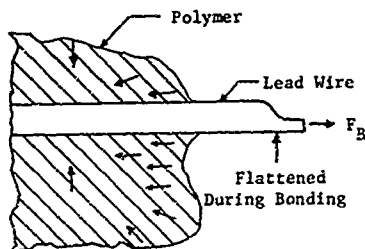


Figure 3.38: Schematic Representation of Forces Developed on Lead Wire by Polymer Compression.

In spite of the device failure--which would have probably occurred sometime during normal (hermetically-sealed) operation with a sufficient vibrational input--the experiment was useful in indicating that the DC 200 was capable of providing a good heat transfer even at 15000 psi. A subsequent check of the 2N3740 mounted on the same circuit board in air, using a 30 volt supply and the same base current drive, gave an initial $I_C = 171$ mA. The transistor heated rapidly and by two minutes I_C had reached 203 mA and was still rising. The polymeric coating over the device started smoking and lifted away, so the experiment was halted. A subsequent curve tracer check revealed that the transistor was still good. This exercise provided a graphic demonstration of the cooling provided by the DC 200 even at 15000 psi.

The data from this test are inconclusive as to whether or not the heat transfer slightly improves with pressure, but they do indicate that substantial cooling occurs due to immersion and that the heat transfer rate is decreased little, if at all, at 15000 psi. This result is very promising for the operation of power dissipating electronic components to the deepest ocean pressures.

4.0 CONCLUSIONS

"Contemporary electronic components will withstand and indeed function at the deepest ocean pressures" - a review of the literature describing the operation of existing outboarded electronic systems is ample proof of this statement. Aside from the fact that there are operational systems which testify to the practicality of outboarded electronics, the literature also indicates that there are also many other devices which have been tested and appear to be outboarding candidates [Ref. 6]. What the literature does not establish is the art, technology and criteria needed to select, reject, apply, and test for potential usefulness. The present study has attempted to uncover some of the fundamental problems and solutions which will be encountered in outboarding contemporary electronic components. The following paragraphs document some of the conclusions from the study.

4.1 Pressure Effects

The first and foremost conclusion is that most electronic materials, metals, semiconductors or dielectrics, are unaffected by either the pressure of interest for ocean use or typical pressure transmitting fluids. This is particularly true for solid forms such as crystals, films, and wires. There is ample proof that these material forms are not sensitive to pure hydrostatic pressures in the range of interest for present or future Naval operations. On the other hand, granular and pressed powdered materials are very sensitive to pressure and consequently components made from these material forms should be avoided.

Non-hydrostatic stresses induced by housings as the result of voids, mismatch in elastic properties and stresses induced at the time of manufacture

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can and often do cause device failures to occur with the electronic materials. In almost all cases for semiconductors and dielectrics, the electronic material will fracture and result in a catastrophic failure as opposed to reusable non-destructive failures. For example, a semiconductor chip may fracture at pressure levels below that which would result in noticeable material property damages when there is a void in the chip-to-substrate bond.

While most electronic materials can be expected to withstand the hydrostatic pressures, the package that contains the active elements may not withstand the pressure. The most common failures are package deformations resulting in the creation of catastrophic stress levels for the enclosed elements. Voids are the number one cause of failure with elastic property mismatch a poor second. The present design of TO cans and thin lid (particularly metal) flat packs makes them unusable for immersed operation. Although some TO cans are usable to several thousand psi (TO-18), most fail well below this. The present variability in such factors as wall thickness, material and edge rounding gives a wide range of maximum allowable pressure for a given type--too wide for any confident statement that, e.g., "TO-3 cans are usable to 500 foot depths."

Some existing ceramic DIP designs will provide pressure resistance to depths nearing the deepest part of the ocean. As in the case of TO-cans, however, variations in material and geometry can give a fairly wide range of maximum allowable pressure. The key to the pressure resistance of present ceramic DIP designs is a relatively small cross-sectional void area and a relatively thick cover.

Plastic packages without internal voids are not subject to catastrophic crushing. However, the relatively large compressibility of plastics

compared to other material may promote deformation which can pull lead wires from semiconductor devices.

Passive component packages follow the same pattern. Solidly filled housings transmit stress directly to components and do not lead to catastrophic failure. Packages with voids, however, generally fail at pressures well below those equivalent to that in the deepest parts of the ocean.

4.2 Fluid Effects

Oils are the most prevalent pressure transmitting fluids. Liquids have been used in passive devices for years and in many applications such as transformers; devices such as resistors are stored in oil with no adverse effects. Oil is in fact a much more benign environment than ordinary air containing moisture. Loss in the fluid can cause device failures, through corrosion or ionic induced effects such as inversion layers in semiconductor devices. The present studies indicate that most semiconductor devices are fabricated in such a manner as to make them impervious to oils in contact with them. This is particularly true for integrated circuits. Experimental evidence also indicates that contamination effects are minimal. Both short and long term studies indicate that bipolar semiconductor devices are not affected.

4.3 Pressure Hardening Techniques

Several schemes are feasible to pressure harden devices. The most obvious technique is to encapsulate the device with enough material with sufficient strength to absorb the pressure and hence protect the device. Epoxy is a good candidate for most devices. The second technique is to change the package geometry. For example, a hemispherical transistor package can withstand almost an order of magnitude more pressure than one with a flat top. The third and by far the most promising is to feed

the device. It may be that a pliable coating of a passivant material may be needed to isolate the fluid from the device, however, initial results on most devices indicate that this is unnecessary.

Several cautions are worthy of mention: (1) make the device as small as possible (stress is force per unit area); (2) choose devices constructed of materials of similar elastic properties; (3) avoid use of manufacturing practices which result in uncontrollable voids in the device at locations which cannot be flooded; and (4) avoid components which utilize liquids, powdered materials, and laminates.

This study has not uncovered any problems that will not be solvable and hence prevent the use of almost all electronic components in an out-boarded mode. This does not imply that there are not numerous problems to be solved. The art and the technology must be discovered and documented on a practical level.

4.4 Reliability

No definitive statement can be made on the whole question of reliability of electronic devices for pressure tolerant electronics at this time. Very few studies have been conducted that have considered enough samples to have any significant statistical value. Almost all investigations, the present study included, have utilized representative devices but often only one or two in each category.

The present study has considered some of the more obvious failure modes. However, subtle failure mechanisms will certainly be identified for all device types. Experimentally, the most common failure mechanisms were those normally encountered in devices, such as voids in the bonding, misplaced leads and poor metallization. The fluid-pressure environment, like mechanical testing, will sometimes accelerate these failure mechanisms.

It should be emphasized that no significant long term testing was done in this study. Although several fluid immersion studies were conducted for as long as one year, the tests were not backed up by adequate control and base line studies to allow statistical evaluations. The most important tests will involve cycling for long periods of time. This approach has been used at NUC, and numerous failures have occurred for some devices.

The whole area of plastic creep and stress relaxation has not been treated and will need much attention. Evaluations of these problems should result in the establishment of needed screening tests for the pressure induced failures. Failure modes that result from the pressure may be more or less difficult to detect than those now encountered. For example, over pressurization may be an excellent accelerated testing method.

From a reliability view, the fact that devices will be free flooded in an inert liquid could greatly enhance their reliability. This is true for two reasons: (1) for free flooded devices the device will often be uncapped or unencapsulated thereby permitting visual inspection even after assembly into such systems; (2) the inert fluid will likely be more benign than the typical encapsulation atmospheres. The latter should greatly reduce the mobility of such impurities as water vapor. Many failure modes are the result of poor quality control of the encapsulating environment.

5.0 RECOMMENDATIONS

Based on the results of this study and the need for Navy systems which will function at deep ocean pressures, the following recommendations are offered:

- A study should be initiated to define feasible approaches to the utilization of devices which are to be free flooded with the pressurizing fluid. This should be coordinated very closely with device manufacturers in order to assure economical feasibility of the technology developed.
- A study should be initiated to develop passivation techniques and materials to protect those devices that are sensitive to the pressurizing fluid and which must be free flooded.
- A study should be initiated to develop potting techniques for those devices that must be protected against the pressure in order to insure that all types of components are available for the systems designers.
- A study should be initiated to evaluate failure mechanisms that are expected, with particular emphasis on those induced by the fluid-pressure environment.

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- A study should be initiated to develop a methodology for evaluation of the reliability of devices and systems in the fluid-pressure environment.
- A study should be initiated to consider modular approaches to be utilized with components for use in the fluid-pressure environment.
- A study should be initiated to develop systems concepts for pressure tolerant electronics.

6.0 APPENDIX

6.1 Fundamental Stress-Strain Relations

The general problem faced in our analysis is to determine the stress distribution $s(x,y,z)$ in a laminar slab of material, thickness t , with a uniform pressure P applied to one surface and a set of reaction forces, R , and force couples (bending moments, M) applied to the periphery. The general case is sketched in Figure 6.1 below.

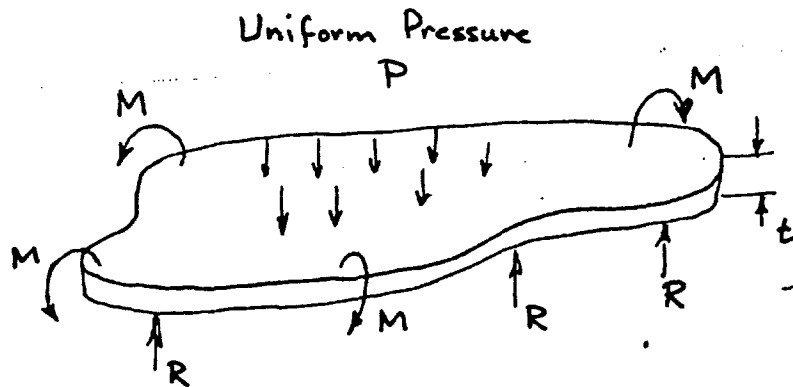


Figure 6.1: Forces and moments applied to laminar slab

In general, the stresses resulting from the force and moment distribution can be specified by the normal stress components s_1 , s_2 and s_3 and the shearing stress components s_4 , s_5 and s_6 . These are shown acting on a volume element of the material in Figure 6.2 [Ref. 11]. The strains resulting from a general stress distribution in the material are specified by considering the change in displacement of a general point (u,v,w) in the body with respect to the origin O of a set of rectangular axes x , y , z . The change in u , v and w along the three coordinate axes $\frac{\partial u}{\partial x}$, $\frac{\partial u}{\partial y}$, $\frac{\partial u}{\partial z}$,

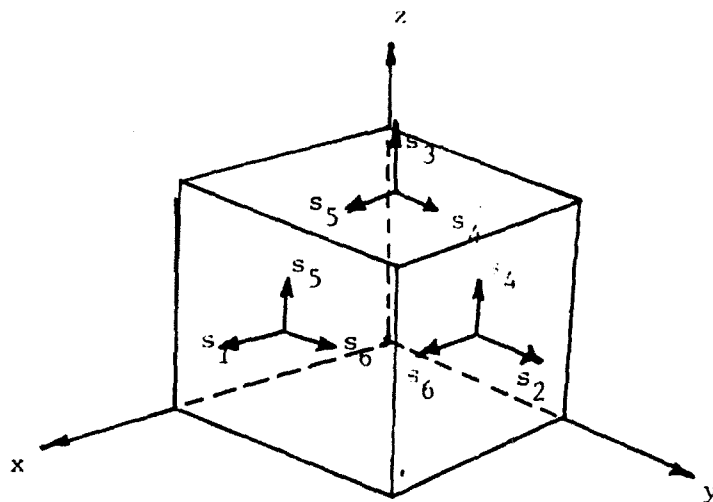


Figure 6.2: Normal and shear stress component.

etc., are used to define the normal strains

$$e_1 \equiv \frac{\partial u}{\partial x}, e_2 \equiv \frac{\partial v}{\partial y}, e_3 \equiv \frac{\partial w}{\partial z}$$

and the shear strains

$$e_6 \equiv \frac{\partial u}{\partial y} + \frac{\partial v}{\partial x}, e_5 \equiv \frac{\partial u}{\partial z} + \frac{\partial w}{\partial x}, e_4 \equiv \frac{\partial v}{\partial z} + \frac{\partial w}{\partial y}.$$

Under the assumptions of linear elastic theory enumerated above, the components of stress and strain are related by

$$s_j = c_{jk} e_k \quad (6.1)$$
$$j, k = 1, 2, 3, 4, 5, 6$$

where the c_{jk} are the elastic constants for the material and the repeated index, k , implies a summation. For the homogeneous, isotropic material assumed there are only three independent values of the c_{jk} coefficients, which are usually designated c_{11} , c_{12} and c_{44} . This reduces the equations implied by 2.4 to the form [Ref. 11]

$$s_1 = c_{11}e_1 + c_{12}(e_2 + e_3) \quad (6.2a)$$

$$s_2 = c_{12}(e_1 + e_3) + c_{11}e_2 \quad (6.2b)$$

$$s_3 = c_{12}(e_1 + e_2) + c_{11}e_3 \quad (6.2c)$$

$$s_4 = c_{44}e_4 \quad (6.2d)$$

$$s_5 = c_{44}e_5 \quad (6.2e)$$

$$s_6 = c_{44}e_6 \quad (6.2f)$$

where

$$c_{11} = (1 - \nu)E/(1 + \nu)(1 - 2\nu) \quad (6.3)$$

$$c_{12} = \nu E/(1 + \nu)(1 - 2\nu) \quad (6.4)$$

$$c_{44} = E/2(1 + \nu) \quad (6.5)$$

where ν is Poisson's ratio and E is Young's modulus.

Given the applied force and moment distributions, the stress distribution may in principle be calculated. The problem is greatly reduced in complexity when there is a high degree of symmetry in the geometry of the body and the applied force distributions, which is true in enough electrical component packages to allow the use of relatively simple formulas to gain sufficient insight into manageable cases to obtain estimates of what will happen in more complicated situations. Formulas for stress in circular and rectangular plates and for cylinders under a uniform distributed load (pressure), among others, have been tabulated by Roark [Ref. 12] and are used wherever possible. For more complicated cases, such as composite material slabs, simple assumptions can be made which allow extension of the formulas. For example, a plate consisting of two different materials can be assumed to have no slippage at the interface.

6.2 Analysis of TO Can Structures

In the case of the TO can, a reasonable mathematical model is to use a cylindrical structure with a flat top to represent the cap of the TO can, and then to use a thick disk to represent the header, or the bottom, of the TO can. With this model, one may then apply formulas

derived for standard cases [Ref. 10], and analyze stresses developed at various parts of the structure due to the influence of an external pressure upon the structure. These formulas are derivable from a more general mathematical treatment of stress and strain, such as obtained from a standard textbook of the theory of elasticity and a brief summary of this theoretical analysis is given in Section 6.1 above.

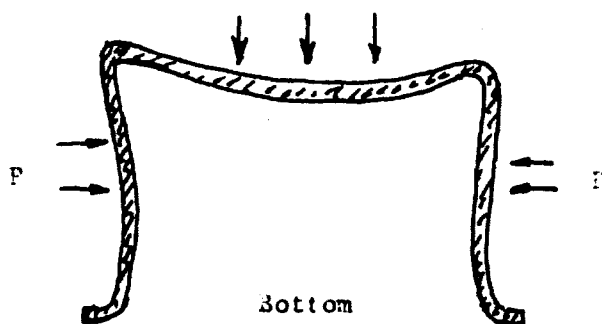
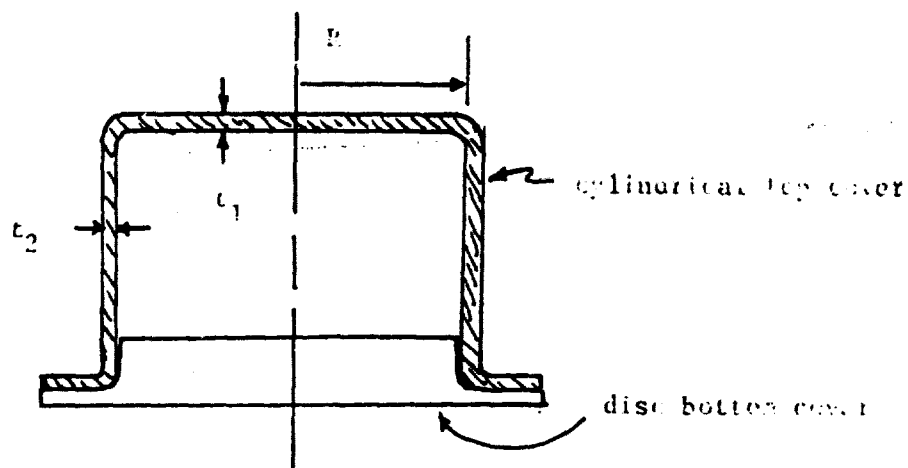
Figure 6.3 shows the model used for a TO can and shows the analysis of this model into a free-body diagram to facilitate the mathematical approach.

The mechanical stresses generated in the cap can be calculated theoretically by using superposition and the free-body diagram which is shown in Figure 6.3. The forces acting upon the cap are membrane forces acting on the flat top and on the cylindrical sides, a shearing force, denoted by V_0 in the diagram, and a bending moment, denoted by M_0 in the diagram. By using the principle of superposition, the effects of each of these separate forces can be calculated on the flat top structure and on the cylindrical structure, and then added together. For the cylinder there are three conditions. There is a condition due to uniform external pressure which results in a meridional membrane stress given by Equation (6.6)

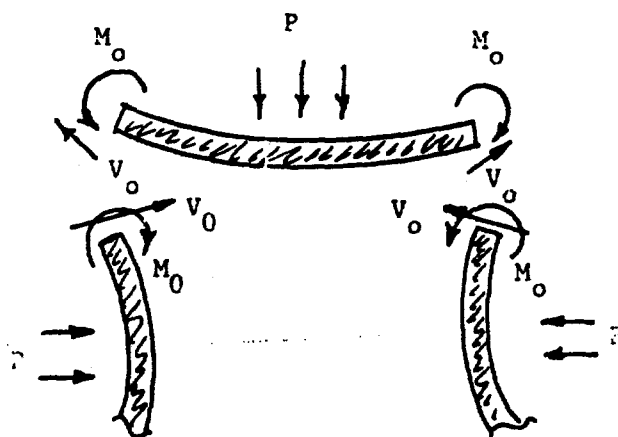
$$s_1 = \text{membrane meridional stress} = -P \frac{R}{2t_2} . \quad (6.6)$$

A stress at right angles to the meridional stress, which is called the "hoop" membrane stress, given by Equation (6.7)

$$s_2 = \text{membrane hoop stress} = -P \frac{R}{t_2} . \quad (6.7)$$



Effect of pressure on
top cover



Free body diagram with imposed
stress system:

P - applied external pressure

M_0 - induced bending moment

V_0 - induced shear

Figure 6.3: Free body diagram for flat top cover
of TO can type housing

The stresses due to the uniform radial shear force, V_o , are the meridional bending stress, which in this case is identically zero at the end,

$$s'_1 = \text{bending meridional stress} = 0 \quad (6.8)$$

and a "hoop" bending stress, which is also identically zero at the end.

$$s'_2 = \text{bending hoop stress} = 0 . \quad (6.9)$$

Also, there is "hoop" membrane stress due to V_o , which is given by Equation (6.10)

$$s_2 = - 2V_o \lambda_2 R / t_2 . \quad (6.10)$$

The stresses due to the uniform radial bending moment, M_o , are a meridional bending stress, given by Equation (6.11), a "hoop" bending stress, given by Equation (6.12), a "hoop" membrane stress, given by Equation (6.13), a shear stress, given by Equation (6.14)

$$s'_1 = 6M_o / t_2^2 \quad (6.11)$$

$$s'_2 = \nu 6M_o / t_2^2 \quad (6.12)$$

$$s_2 = - 2M_o \lambda_2^2 R / t_2 \quad (6.13)$$

$$s_5 = V_o / t . \quad (6.14)$$

The stresses in the cap due to membrane effects, the shearing force, and the bending moment are a tangential stress, given by Equation (6.15); a radial stress due to the bending moment, M_o , which is given by Equation (6.16); and a tangential stress, due also to the bending moment, given by

Equation (6.17). Finally, due to the shear moment, V_o , there is developed a uniform radial stress given by Equation (6.18)

$$s_t = -\frac{3R^2}{4t_1^2} (1/2 - 1) P \quad (6.15)$$

$$s_r = 6M_o/t_1^2 \quad (6.16)$$

$$s_t = 6M_o/t_1^2 \quad (6.17)$$

$$s_r = V_o/t_1 \quad (6.18)$$

Matching the boundary conditions and solving for the bending moment, M_o , and the shearing force, V_o , gives the formulas for these two quantities shown below in Equations (6.19) and (6.20).

$$M_o = \left[\frac{\frac{R^3 \lambda_2^2 D_2}{4D_1(1+\nu)} + \frac{2R^2 \lambda_2^2 t_1 D_2}{t_2(1-\nu/2)[Et_1 + 2RD_2 \lambda_2^3(1-\nu)]}}{2 + \frac{2R \lambda_2^2 D_2}{D_1(1+\nu)} - \frac{Et_1}{Et_2 + 2D_2 R \lambda_2^3(1-\nu)}} \right] P \quad (6.19)$$

$$V_o = 2\lambda_2 \left[1 + \frac{R \lambda_2^2 D_2}{D_1(1+\nu)} \right] M_o - \left(\frac{R^3 \lambda_2^2 D_2}{4D_1(1+\nu)} \right) P \quad (6.20)$$

The parameters, λ and D , with a subscript 1 appropriate for the top of the cap, and subscript 2 appropriate for the cylindrical side of the cap, are given in Equations (6.21) and (6.22) below.

$$D_k = \frac{Et_k^3}{12(1-\nu^2)} \quad k = 1, 2 \quad (6.21)$$

$$\lambda_k = \left[\frac{3(1-\nu^2)}{R^2 t_k^2} \right]^{1/4} \quad k = 1, 2 \quad (6.22)$$

For convenience, these formulas are summarized in Table 6.1 and Table 6.2.

To give an example of the use of these formulas for an analysis, a typical calculation is made in the following.

Example:

TO-18

Material: Nickel

$R = 0.088$ in

$t_2 = 0.00775$ in

$t_1 = 0.0095$ in

$E = 4 \times 10^7$ psi

$\nu = 0.28$

$m = 1/\nu = 3.57$

Cylinder

	P	V_o	M_o
s_1	-5.7P	0	0
s'_1	0		-79.8P
s_2	-11.3P	53.8P	-44.2P
s'_2	0	0	22.3P
s_3	0	6.19P	0

The sum of the meridional stresses on the outside gives

$$s_1 + s'_1 = 74.1P$$

Table 6.1: Flat top cylinder treatment - cylinder stress components

Stress \ Cause	P	v_c	M_o
s_1	$-\frac{PR}{2t_2}$	0	0
s'_1	0	0	$+\frac{6M_o}{t_2^2}$ $-\frac{6M_o}{t_2^2}$
s_2	$-\frac{PR}{t_2}$	$-\frac{2v_o \lambda R}{t_2}$	$-\frac{2M_o \lambda^2 R}{t_2}$
s'_2	0	0	$+\frac{6M_o}{t_2^2}$ $-\frac{6M_o}{t_2^2}$
s_s	0	$\frac{v_o}{t_2}$	0

Table 6.2: Disc Stress Components

	Stress \ Cause	P	v_o	M_o
Edge	s_r	0	$\frac{v_o}{t_1}$	$+\frac{6M_o}{t_1^2}$ $-\frac{6M_o}{t_1^2}$
	s_t	$-\frac{3R^2}{4t_1^2} (1-\nu) P$	0	$+\frac{6M_o}{t_1^2}$ $-\frac{6M_o}{t_1^2}$
Center	s_r	$-\frac{3R^2}{4t_1^2} (3-\nu) P$	$\frac{v_o}{t_1}$	$+\frac{6M_o}{t_1^2}$ $-\frac{6M_o}{t_1^2}$
	s_t	$-\frac{3R^2}{8t_1^2} (3+\nu) P$	0	$+\frac{6M_o}{t_1^2}$ $-\frac{6M_o}{t_1^2}$

The sum of the meridional stresses on the inside wall is

$$(s_1 + s_1') = -85.5P .$$

The sum of the hoop stresses on the outside wall is

$$(s_2 + s_2') = 20.6P .$$

The sum of the hoop stresses on the inside wall is

$$(s_2 + s_2') = -24.0P .$$

The maximum stress experienced in the cylinder is therefore:

$$(s_1 + s_1') = -85.5P .$$

For a yield stress of 20,000 psi for nickel

$$P = 234 \text{ psi}$$

	Head		
	P	M _o	V _o
s _r		53P	-5.0P
s _t	-46.4P	53P	0

The maximum stress in the top is

$$s_r = 48P .$$

In practice, a perfectly flat-top cylinder is seldom encountered. Usually, the sides are rounded to some extent. In some cases, the rounding

approaches a hemispherical surface. To obtain an idea of how such rounding will affect the stress resistance of the structure, one may take the limiting case of a cylinder surmounted by a hemisphere and perform a calculation in a manner similar to that performed above. Again, using standard formulas from Roark [Ref. 12, pg. 307]. In particular, we take the special case where the top thickness, t_1 , of the hemispherical top is equal to the side thickness, t_2 , of the cylindrical side. In this case, the bending moment is equal to zero, and the shear force, V_0 lbs per linear inch, is given by Equation (6.23) below.

$$V_0 = P/8\lambda_1. \quad (6.23)$$

The membrane forces on the hemispherical top are given by Equation (6.24) below.

$$s_1 = s_2 = PR/2t. \quad (6.24)$$

The stresses due to the shear, V_0 , are a stress of zero magnitude in a meridional direction at the edge, and a hoop membrane stress given by Equation (6.25) below.

$$s_2 = \frac{2V_0}{t} \left[3(1 - \nu^2) \left(\frac{R}{t} \right)^2 \right]^{1/4}. \quad (6.25)$$

The stresses in the cylinder are given by the stresses previously quoted, so that now the appropriate values of bending moment, M_0 , which is zero in this case, and a formula for the shear force, V_0 , can be used to calculate the stresses which developed in the cylindrical sides and

the hemispherical top under the influence of an external pressure, P . These formulas are summarized in Tables 6.3 and 6.4. A comparison calculation of the maximum operating depths for several common TO can types with a flat top and with a hemispherical top are given in Table 6.5.

Table 6.3

Hemispherical cap treatment for equal side and top thicknesses
Cylinder stress Components

Stress \ Cause	P	V_o	M_o
s_1	$- PR/2t$	0	0
s'_1	0	0	0
s_2	$- PR/t$	$- PR/4t$	0
s'_2	0	0	0
s_0	0	$P/8\lambda t$	0

Table 6.4

Hemispherical cap stress components

Stress \ Cause	P	V_o	M_o
s_1	$- PR/2t$	0	0
s_2	$- PR/2t$		0

Table 6.5: Comparison of maximum operating depths for some common TO can types with flat tops and with hemispherical tops

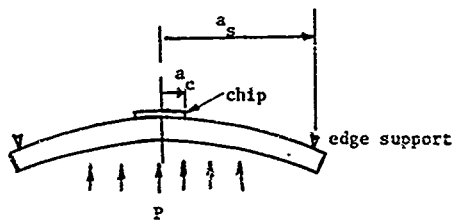
TO Can Type	<u>Maximum Operating Depth (ft)</u>	
	<u>Flat Top</u>	<u>Hemispherical Top</u>
TO-18.	843	7700
TO- 5	550	6500
TO-66	248	2730
TO- 3	92.4	1670
TO-36	114	1870

6.3 Analysis of Semiconductor Chip Fracture Due to Header Deformation

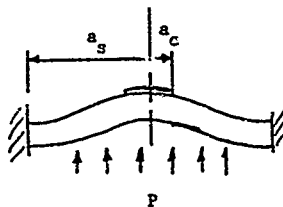
The situation at the header or the bottom cover of the cap under pressure is analyzed by considering two possible cases. These cases are sketched in Figure 6.4. One possibility is that the edge of the header is supported by the cap, but is free to bend. For this model we will assume a circular semiconductor chip with radius a_c , bonded to a circular substrate with radius a_s . The substrate or header is deformed by an external pressure, P , acting on the bottom of the surface, which causes a deflection of the header about the fixed edge supports. We also assume that in the bending, the semiconductor chip does not stiffen the substrate in any way. From [Ref. 12, pg. 216], the maximum deflection and maximum stress will occur at the center, and the value of this maximum stress is given by Equation (6.26) below:

$$s_m = (s_r)_{\max} = (s_t)_{\max} = \frac{3}{8} \left(\frac{a_s}{t} \right)^2 (3 + \nu_s) P . \quad (6.26)$$

This maximum stress is developed at the extreme fiber edges or the upper surface of the header and is in tension. The lower surface of the header



Case 1: edges supported, but not clamped.



Case 2: edges clamped.

Figure 6.4: Header under pressure

is, of course, in compression. The stress and strain for a homogeneous header are related by formulas (6.27) and (6.28) for the two strain components, and these formulas are given below:

$$e_r = \frac{1}{E_s} (s_r - \nu_s s_t) \quad (6.27)$$

$$e_t = \frac{1}{E_s} (s_t - \nu_s s_r) \quad (6.28)$$

At the center, where the two strain components are equal, their value is given as a function of z , z being the vertical axis to the center of the header, as (6.29) below:

$$e_r = e_t = \frac{2s_m}{t} \left(\frac{1 - \nu_s}{E_s} \right) z \quad (6.29)$$

We take the $z = 0$ to be the position of the neutral axis or the axis of zero strain through the header. If it is now assumed that the strain is transmitted to the chip without slippage at the interface (perfect bond), the maximum strain will occur in the upper surface of the chip. The value of this strain is given by Equation (6.30) below:

$$e_{mc} = \frac{2s_m}{t} \left(t/2 + t_c \right) \left(\frac{1 - \nu_s}{E_s} \right) \quad (6.30)$$

Since

$$s_{mc} = \frac{E_c}{(1 - \nu_c)} e_{mc} \quad (6.31)$$

$$s_{mc} = \left(\frac{E_c}{E_s} \right) \left(\frac{1 - \nu_s}{1 - \nu_c} \right) \left(1 + \frac{2tc}{t} \frac{3}{8} \frac{a}{t} \right)^2 (3 + \nu_s) P \quad (6.32)$$

Take, for example, a Kovar substrate which has the values 0.28 for Poisson's ratio and 2×10^7 psi for the elastic constant, E_s , with a radius $A_s = .150$ inches and a thickness, t , equal to .060 inches. These dimensions are obtained for a typical can type TO-5 header. For a typical silicon chip whose dimensions are: $a_c = .030$ inches and a thickness, $t_c = .010$ inches, and assuming the values 0.27 for Poisson's ratio and 1.83×10^7 psi for the modulus elasticity, E_c . We calculate from Formula (6.32) that the maximum stress developed at the upper surface of the chip has the value given by Equation (6.33) below:

$$s_{mc} = 9.37 P . \quad (6.33)$$

The maximum allowable stress in silicon in bending is given by [Ref. 13] as 5.07×10^4 psi. Using the result of Equation (6.33), this stress, the maximum allowable stress, is developed at a pressure of 5400 psi.

The second extreme case for the header is to assume that the cap holds the edges of the header rigidly so that they are fixed and not allowed to bend only if the circular interior of the header is allowed to bend. Again, we assume that the semiconductor chip does not affect the substrate bending. We again assume that the strain of the upper surface of the header is transmitted to the chip without slippage at the interface. Using the formula given by Roark [Ref. 12, p. 217], the stress developed at the center of the base is given by Equation (6.34):

$$s_m = s_r = s_t = \frac{3(1 + \nu_s)}{8} \left(\frac{a_s}{t} \right)^2 P . \quad (6.34)$$

The stress and strain for a homogeneous substrate are related by Equations (6.35) and (6.36):

$$\epsilon_x = \frac{1}{E_s} (\sigma_x - \nu_s \sigma_z) \quad (6.35)$$

$$\epsilon_z = \frac{1}{E_s} (\sigma_z - \nu_s \sigma_x) \quad (6.36)$$

At the center where the two strain components are equal, the strain is given by Equation (6.37) with $z = 0$, taken at the neutral axis.

$$\epsilon(0, z) = \frac{2s_m}{t} \left(\frac{1 - \nu_s}{E_s} \right) z \quad (6.37)$$

The strain at the upper surface of the chip is given by Equation (6.38):

$$\epsilon_{mc} = \frac{2s_m}{t} (t/2 + t_c) \left(\frac{1 - \nu_s}{E_s} \right) \quad (6.38)$$

Since

$$s_{mc} = \frac{E_c}{1 - \nu_c} \epsilon_{mc}$$

$$s_{mc} = \left(\frac{E_c}{E_s} \right) \left(\frac{1 - \nu_s}{1 - \nu_c} \right) \left(1 + \frac{2t_c}{t} \right) \frac{3}{8} (1 + \nu_s) \left(\frac{s}{t} \right)^2 P \quad (6.39)$$

For the same materials and dimensions as in the previous calculation, the maximum stress developed in the chip is related to the pressure by Equation (6.40):

$$s_{mc} = 3.65 P \quad (6.40)$$

Again using a maximum allowable stress in the silicon of 5.07×10^4 psi [Ref. 21], we find that the maximum allowable pressure of operation for a header is 13,900 psi.

It can be seen from the preceding analysis that even if the tops of the TO cans can be reinforced to withstand higher pressures, there still may be dangerous stress levels developed in the silicon chip by deformation of the header. The problem of a composite header made of glass and metal combined can be approached by modifying the equations for the single material case.

For a model, we take the fixed edge case which has already been analyzed above, and we modify it to the case of the composite material. The formula which gives the maximum stress, S_m , has already been quoted above as formula (2.32). In this analysis, we will assume that there is no slippage of any material interface. We will assume that the presence of the semiconductor chip does not influence the stiffness of the header disk, we will assume that there are only small deflections, and we will further assume that there is a linear strain relation. Because of the linearity of strain and therefore of the stress, the stress as a function of z is given by Equation (6.41):

$$s(0,z) = s_m \frac{2z}{t} . \quad (6.41)$$

The bending moment per unit length at the center of the disk, M , is equal to zero, and is given by Equation (6.42):

$$M = s_m \int_{-t/2}^{t/2} \frac{2z^2}{t} dz = \frac{4s_m}{3t} (t/2)^3$$

$$M = \frac{2}{3} (t/2)^2 \times \frac{3}{8} \left(\frac{a}{t} \right)^2 (1 + \nu) P$$

$$M = \frac{a^2}{16} (1 + \nu) P . \quad (6.42)$$

Note that this is the bending moment in one direction only. The factor ν , Poisson's ratio, takes into account the lateral effects in the material and hence, is a material dependent property. However, for most materials, the value of ν lies between 0.25 and 0.30 with 0.28 being a representative value. Therefore, to first order the bending moment is independent of the material, and for a given P will depend only on the overall dimensions. For the model composite disk, the assumed linear strain is given by Equation (6.43), where the slope, α , is to be determined.

$$e(0, z) = \alpha z . \quad (6.43)$$

Let z_0 be the boundary between the material 1 and material 2. Then the sum of the applied forces must be equal to zero and is given in Equation (6.44)

$$F = 0 = \int_{-(t_2 - z_0)}^{t/2} \frac{E_2 \alpha}{1 - \nu_2} z dz + \int_{z_0}^{t_1 + z_0} \frac{E_1 \alpha}{1 - \nu_1} z dz$$

$$0 = \frac{E_2 \alpha}{2(1 - \nu_2)} [z_0^2 - (t_2 - z_0)^2] + \frac{E_1 \alpha}{2(1 - \nu_1)} [(t_1 + z_0)^2 - z_0^2] . \quad (6.4)$$

Divide by $E_1 \alpha / 2(1 - \nu_1)$ and set $\Lambda = E_2(1 - \nu_1) / E_1(1 - \nu_2)$. Now,

$$\Lambda(2z_0 - t_2)t_2 + t_1(2z_0 + t_1) = 0 ,$$

or

$$z_0 = (\Lambda t_2^2 - t_1^2) / 2(\Lambda t_2 + t_1) \quad (6.45)$$

Therefore, the position of the neutral axis is determined by the relative thicknesses, and the material constants. The applied moment is given by Equation (6.46), which reduces to the value given by Equation (6.47).

$$M = \int_{-(t_2-z_0)}^{z_0} \frac{E_2 \alpha}{1-\nu_2} z^2 dz + \int_{z_0}^{t_1+z_0} \frac{E_1 \alpha}{1-\nu_1} z^2 dz \quad (6.46)$$

$$M = \frac{E_2 \alpha}{3(1-\nu_2)} [t_2^3 + (t_2-z_0)^3] + \frac{E_1 \alpha}{3(1-\nu_1)} [(t_1+z_0)^3 - z_0^3] \quad (6.47)$$

Solving for the slope factor, α , and using Equation (6.42) for the value of M , we find that α is given by Equation (6.48):

$$\alpha = \frac{3}{16} \frac{a_s^2 (1+\nu) P}{\frac{E_2 [t_2^3 + (t_2-z_0)^3]}{1-\nu_2} + \frac{E_1 [(t_1+z_0)^3 - z_0^3]}{1-\nu_1}} \quad (6.48)$$

Taking as a typical example a Veritron West JEDEC TO-5 shell-type material seal with

Kovar	{	$E_1 = 2 \times 10^7 \text{ psi}$	$t_1 = 0.015 \text{ inches}$
		$\nu_1 = 0.28$	$a_s = 0.300 \text{ inches}$
Glass	{	$E_2 = 1.5 \times 10^7 \text{ psi}$	$t_2 = 0.085 \text{ inches}$
		$\nu_2 = 0.25$	$a_s = 0.300 \text{ inches}$

then $A = 6.782$ and from (2.43), $z_0 = 3.34 \times 10^{-2} \text{ inches}$.

The upper limit of $z = t_1 + z_0 = 48.4$ mils. The lower limit of $z = -(t_2 - z_0) = -51.6$ mils. Therefore, the neutral axis is displaced from the center line slightly toward the Kovar. The slope of the strain curve is

$$\alpha = \frac{3}{16} \frac{(0.3)^2 (1.28) P}{\frac{15[(8.5)^3 + (8.5 - 3.34)^3]}{0.75} + \frac{20[(1.5 - 3.34)^3 - (3.34)^3]}{0.72}}$$

$$\alpha = 1.26 \times 10^{-6} P . \quad (6.49)$$

The maximum tensile strain in the Kovar is given by

$$(e_{\max})_{\text{Kovar}} = 1.26 \times 10^{-6} \times .0464 P = 6.09 \times 10^{-8} P . \quad (6.50)$$

At $P = 1.5 \times 10^4$ psi, $e_{\max} = 9.13 \times 10^{-4}$. This corresponds to a stress in the Kovar of

$$(s_{\max})_{\text{Kovar}} = \frac{2 \times 10^7}{1 - 0.28} \times 9.13 \times 10^{-4} = 2.54 \times 10^4 \text{ psi} .$$

This is about half of the yield stress.

For a 10 mil thick chip of the deformed header, the maximum strain is

$$(e_{\max})_{\text{Si}} = 9.13 \times 10^{-4} \times \frac{.0584}{.0484} = 1.11 \times 10^{-3} .$$

The maximum stress in the silicon chip will be

$$(s_{\max})_{\text{Si}} = \frac{1.83 \times 10^7}{0.73} \times 1.11 \times 10^{-3} = 2.78 \times 10^3 \text{ psi} .$$

The maximum allowable stress in silicon is on the order of 5×10^4 psi, which is about twice the developed stress.

6.4 Analysis of Flat Packs

An indication of the unsuitability of "as is" flat pack designs for operation under pressure is given by considering several examples. The smallest area for the development of a force under pressure is offered by a 1/4" x 1/8" flat pack. Figure 2.12 shows a typical example of this type. The base material is of either metal, alumina or beryllium oxide with a thickness of about 0.02 inches. For these materials, the strengths of interest are:

Metal (Kovar) - yield strength - 5×10^4 psi,

Beryllia - flexural strength - 3.3×10^4 psi,

Alumina - flexural strength - 4.4×10^4 psi.

The base will have an unsupported area of about .087" x 0.197". Taking the formula (2.2) obtained from Reark [Ref. 12, p. 227], with $\beta = 0.5$, the lowest strength material, beryllia, will start to yield at a pressure of

$$P_{\max} = 2 \times 3.3 \times 10^4 \times \frac{.020}{.087}^2 = 13,900 \text{ psi.}$$

However, the top cover plate is typically Kovar of about 0.005" thickness over an unsupported area of 0.107" x 0.217". Therefore, the maximum pressure is limited by this cover to

$$P_{\max} = 2 \times 5.0 \times 10^4 \times \frac{.005}{.107}^2 = 218 \text{ psi,}$$

or an equivalent depth of 419 feet.

Another commonly used flat pack is the 1/4" x 1/4", TO-86. A typical example, manufactured by Texas Instruments, is shown in Figure 2.10. Two

different lid thicknesses are used, 0.0035" and 0.005". If these are made of Kovar, the maximum permissible pressures for the unsupported area of 0.180" x 0.180" are

$$P_{\max} = 63 \text{ psi},$$

or an equivalent depth of about 140 feet, for the thin lid (0.0035") and $P_{\max} = 129 \text{ psi}$ for the "thick" lid (0.005"), or an equivalent depth of 290 feet.

Table 6.6 tabulates these calculated maximum pressures and those for some other commonly used flat pack sizes. Note that in each case, doubling the lid thickness will provide four times as great a maximum allowable pressure. Similar calculations can be made for dual-in-line packages(DIP) which have a flat pack type chip cavity and use, typically, metal lids on the order of 0.010" thick. Several of these are shown in Figure 2.11.

Table 6.6: Maximum allowable operating pressures for
some commonly used flat pack styles

Type	a	b	Lid Thickness (in)	Lid Material	P_{\max} (psi)	Maximum Depth (ft)
1/4" x 1/8"	.217	.107	.005	Kovar	218	490
1/4" x 1/4"	.180	.180	.0035	Kovar	63	142
			.005	Kovar	129	290
1/4" x 3/8"	.315	.200	.010	Kovar	268	604
3/8" x 3/8"	.300	.300	.010	Kovar	180	405

6.5 Passive Component Package Analysis

An understanding of the effects of hydrostatic pressure on passive component packages is provided by consideration of the basic cylindrical package, shown in Figure 6.5. Also shown in this figure is the free body diagram for the forces acting due to hydrostatic pressure P.

Considering the cylinder, it will be assumed that the end pieces are very thick ($t_1 \rightarrow \infty$). In this case, the formulas from case 30, Table XIII, pg. 307 in [Ref. 12] reduce to a bending moment of

$$M_0 = -2PR^2 \lambda_2^2 D_2 / Et_2 (1 - \nu/2) \quad (6.51)$$

and a shear force

$$V_0 = 2\lambda_2 M_0 \quad (6.52)$$

at the ends. In these formulas

$$\lambda_2 = [3(1 - \nu)/R^2 t_2^2]^{1/4} \quad (6.53)$$

$$D_2 = Et_2^3 / 12(1 - \nu^2) \quad (6.54)$$

Denoting by subscript 1 longitudinal stress components and by subscript 2 meridional stress components, the appropriate formulas for the outer surface are:

Membrane stress components:

$$s_1 = \frac{R}{2t_2} P$$

$$s_2 = \frac{R}{t_2} P$$

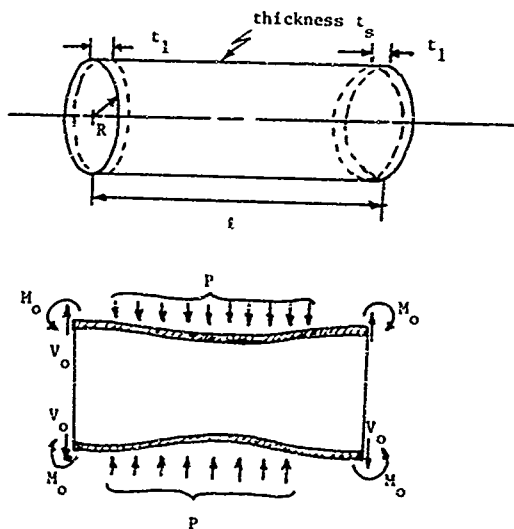


Figure 6.5: Cylindrical component housing

Shear Force Generated Components:

$$s_1' = \frac{6V_o}{\lambda_2 t_2} e^{-\lambda_2 x} \sin \lambda_2 x \quad s_2' = v s_1'$$

$$s_2 = \frac{2\lambda_2^2 R H_o}{t_2} e^{-\lambda_2 x} (\cos \lambda_2 x - \sin \lambda_2 x)$$

The formulas for the shear force and bending moment generated stresses are for one end only ($x = 0$). The same formulas apply to the other end substituting $(l-x)$ for x . Using the principles of superposition, the stress components are added to obtain

$$\begin{aligned} (s_1)_{\text{Total}} &= \frac{-R}{2t_2} + \frac{6V_o}{\lambda_2 t_2} \left[e^{-\lambda_2 x} \sin \lambda_2 x + e^{-\lambda_2 (l-x)} \sin \lambda_2 (l-x) \right] \\ &\quad - \frac{6H_o}{t_2} \left\{ e^{-\lambda_2 x} [\cos \lambda_2 x + \sin \lambda_2 x] \right. \\ &\quad \left. + e^{-\lambda_2 (l-x)} [\cos \lambda_2 (l-x) + \sin \lambda_2 (l-x)] \right\} \quad (6.55) \end{aligned}$$

$$\begin{aligned} (s_2)_{\text{Total}} &= \frac{-R}{2t_2} P + e^{-\lambda_2 x} \left[\left(\frac{6vV_o}{\lambda_2 t_2} \right) \sin \lambda_2 x - \left(\frac{2\lambda_2 R V_o}{t_2} \right) \cos \lambda_2 x \right] \\ &\quad + e^{-\lambda_2 (l-x)} \left[\left(\frac{6vV_o}{\lambda_2 t_2} \right) \sin \lambda_2 (l-x) - \left(\frac{2\lambda_2 R V_o}{t_2} \right) \cos \lambda_2 (l-x) \right] \\ &\quad + \frac{2\lambda_2^2 R H_o}{t_2} \left\{ e^{-\lambda_2 x} [\cos \lambda_2 x - \sin \lambda_2 x] \right. \\ &\quad \left. + e^{-\lambda_2 (l-x)} [\cos \lambda_2 (l-x) - \sin \lambda_2 (l-x)] \right\} \end{aligned}$$

$$-\frac{6\nu M_0}{t_2^2} \left\{ e^{-\lambda_2 x} [\cos \lambda_2 x + \sin \lambda_2 x] + e^{-\lambda_2 x(l-x)} [\cos \lambda_2(l-x) + \sin \lambda_2(l-x)] \right\} . \quad (6.56)$$

The parameter λ_2 is the standard by which the cylinder can be judged to be short or long. For short cylinders (λ_2 small) the end conditions have an appreciable affect near the center of the cylinder ($x = l/2$). For long cylinders, the end effects become negligible approaching the center of the cylinder because of the exponential factors $\exp(-\lambda x)$ and $\exp[-\lambda(l-x)]$.

The formulas (6.55) and (6.56) can be applied to the case of an aluminum housing for an electrolytic capacitor. Typical dimensions are: length, 1-7/8 inches; diameter, 7/8 inches and thickness, 0.015 inches. For aluminum $E = 1 \times 10^7$ psi, $\nu = 0.33$ and the yield stress is $s_y = 2 \times 10^4$ psi. For these values

$$\lambda_2 = [3(1 - 0.11)/(0.438 \times 0.015)^2]^{1/4} = 15.7 \text{ in}^{-1} .$$

This relatively large value of λ allows the neglect of end conditions near the center, and the neglect of conditions at one end when analyzing the stress conditions at the other end. At the center, the stresses are approximately,

$$s_1 = -\frac{0.438}{2(0.015)} P = -14.6 P .$$

$$s_2 = 2s_1 = -29.2 P .$$

The outer surface is in compression with a maximum stress in the meridional ("hoop") direction of about 29 times the applied pressure.

The maximum value of $(s_1)_{\text{Total}}$ occurs at the ends of the cylinder where

$$(s_1)_{\text{Total}} = -14.6 P + 71 P = 56.4 P \quad (x=0, l)$$

i.e., the longitudinal stress is tensile. The value of $(s_2)_{\text{Total}}$ at the ends is also tensile at a maximum value of

$$(s_2)_{\text{Total}} = 32 P, \quad (x=0, l)$$

The critical stress is the longitudinal stress at the ends. Setting this equal to the yield stress $s_y = 2 \times 10^4$ psi gives a maximum pressure of

$$P_{\text{max}} = 2 \times 10^4 / 56.4 = 355 \text{ psi},$$

or an equivalent depth of about 800 feet. Beyond this depth, deformation will start occurring at the ends.

6.6 Effect of Stress on Semiconductors

Intrinsic semiconductor properties are determined to a large extent by the energy band structure of the material. The band shape, position in momentum space, magnitude of energy, and number of band edge points determine the semiconductor properties. It is usually assumed in the energy band model of the piezjunction effect that only the energy separation between the valence band maximum and the conduction band minimum are affected by stress. It is possible to consider some of the other effects such as the change in mobility due to relative population and depopulation of certain energy extremes, and change in effective mass due to the band distortion. However, most of the first order effects of stress on the electrical properties of p-n junctions can be explained by considering only the effective band gap changes.

In general, semiconductors have more than one valence and conduction band edge point. Often the conduction band edge points are not located at the center of the Brillouin zone. Let us consider the general case of α conduction band minima and β valence band maxima. Neglecting any effects of stress on the effective mass and considering the change in the energy levels it can be shown that under stress the minority carrier density, p_n or n_p , is [Ref. 25]

$$\frac{p_n}{p_{no}} = \frac{n_p}{n_{po}} = \frac{1}{\Omega\beta} \left[\exp\left(-\frac{\Delta E_{V1}}{kT}\right) + \exp\left(-\frac{\Delta E_{V2}}{kT}\right) + \dots + \exp\left(-\frac{\Delta E_{V\beta}}{kT}\right) \right] \quad (6.57)$$

$$\times \left[\exp\left(\frac{\Delta E_{C1}}{kT}\right) + \exp\left(\frac{\Delta E_{C2}}{kT}\right) + \dots + \exp\left(\frac{\Delta E_{C\alpha}}{kT}\right) \right] = \gamma_v(e).$$

Where $v = \Omega\beta$ and the ΔE 's are the changes in the respective energy extremes and p_{no} and n_{po} are the zero stress values of minority carrier

density. It is easily shown that the intrinsic carrier concentration is

$$n_i^2 = n_{i0}^2 \gamma_v(e) \quad (6.58)$$

where n_{i0} is the unstressed intrinsic carrier density. The factor $\gamma_v(e)$ is the parameter which relates the carrier density to the change of energy band structure with stress. The number of bands, their energy value, the orientation of the stress with respect to the crystal axis, and the amount of doping influence the dependence of $\gamma_v(e)$ with stress. This dependence is discussed for the various semiconductor materials in the later sections of this report.

Given a particular semiconductor and stress orientation, the ultimate interest lies in the effects of the strain induced changes in the minority carrier density which influence the p-n junction parameters. There are two types of current that flow in p-n junctions: (1) diffusion or ideal current across the space charge region of the junction and (2) generation-recombination current resulting from trap centers in and close to the space charge region of the junction. The generation-recombination current can be separated into two components: (a) that occurring in the bulk material and (b) that occurring at surface of the material. Very little information is available on the effects of stress on the surface current. The effects of stress on the diffusion currents and the bulk generation-recombination currents can be tested.

It is interesting to note that it is the stress at the edges of the depletion region that influences the diffusion currents and not the stress in the depletion region. In a junction with a strain e_n on the n-side of the junction and a strain e_p on the p-side, the hole and electron diffusion currents at a constant bias voltage are [Ref. 25]

$$I_p = I_{p0} \gamma_v(e_n) \quad (6.59)$$

$$I_n = I_{n0} \gamma_v(e_p), \quad (6.60)$$

where e_n and e_p are the general strains at the two sides of the junction and I_{p0} and I_{n0} are the unstressed currents (each are voltage dependent). It is not unusual to introduce stresses in a junction such that one side of the junction is stressed with a larger magnitude than the other. This is particularly true for stress applied with indenter points. The total saturation diffusion current is

$$I_s = I_{p0} \gamma_v(e_n) + I_{n0} \gamma_v(e_p) \quad (6.61)$$

and

$$I_I = I_s (e^{qV/kT} - 1) \quad (6.62)$$

where I_I is the diode diffusion current.

If only a part of the junction area, A , is stressed, for example A_{sn} on the n-side and A_{sp} on the p-side, as shown in Figure 6.6,

$$I_s = I_{p0} \left[\frac{A - A_{sn}}{A} + \frac{1}{A} \int_{A_{sn}} \gamma_v(e_n) dA_{sn} \right] \\ + I_{n0} \left[\frac{A - A_{sp}}{A} + \frac{1}{A} \int_{A_{sp}} \gamma_v(e_p) dA_{sp} \right] \quad (6.63)$$

For the special case of uniform strain ϵ

$$I_s = I_{s0} \left[\frac{A - A_s}{A} + \frac{A_s \gamma_v(\epsilon)}{A} \right] \quad (6.64)$$

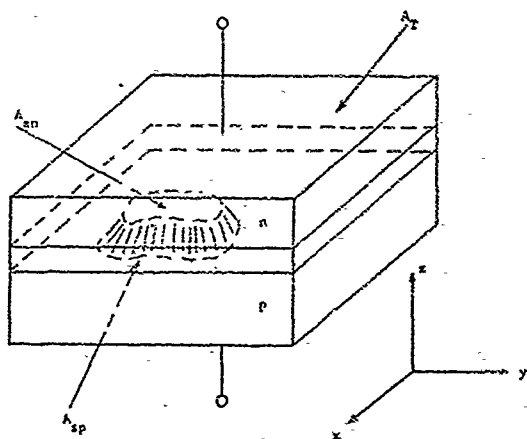


Figure 6.6A: Stressed p-n junction model. [Ref. 25]

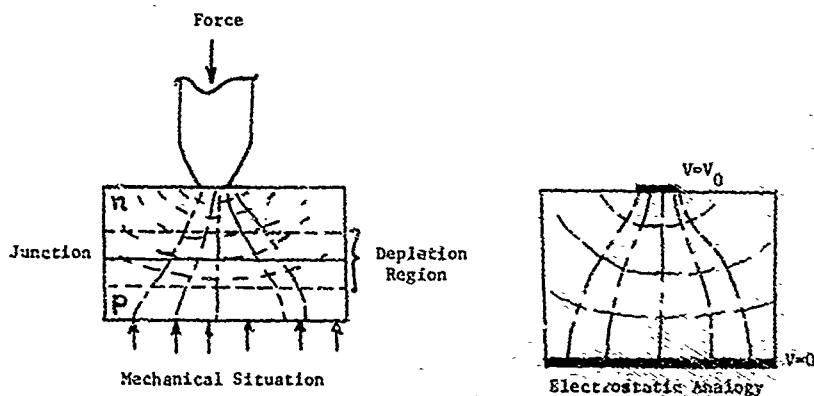


Figure 6.6B: Stress situation with a different stress distribution at n-side of depletion region than at the p-side of the depletion region.

In the case of bulk generation-recombination currents, it is the stress in the junction that affects the current. The recombination current is given by

$$I_r = \frac{a \gamma_v(n)^{1/2} (e^{qV/kT} - 1) (V - V_0)^{1/2}}{1 + b e^{qV/2kT}} \quad (6.65)$$

where a and b are constants depending on the lifetime and number of trap centers and their energy positions in the band gap, and V_0 is the built-in junction potential. This expression neglects changes in the trap energy. The effects of stressing only a part of the junction can be accounted for in the same manner as was done for the diffusion current.

6.6.1 Effect of Stress on Ge and Si

The effect of stress on Ge and Si has been previously reported. The following is a summary of the previous work [Refs. 25, 26, 27] and is included for completeness of this report.

The energy band structures of Ge and Si are shown in Figures 6.7 and 6.8. The degenerate Γ'_{25} level located at $k = (000)$ is the maximum valence level and is assigned an energy value of zero for both Ge and Si. Actually Γ'_{25} has two different energy values, one corresponding to $j = \frac{1}{2}$ and one corresponding to $j = \frac{3}{2}$. The Γ'_{25} ($j = \frac{1}{2}$) level is ~ 0.04 eV below the Γ'_{25} ($j = \frac{3}{2}$) level for Si and ~ 0.3 eV for Ge. The Γ'_{25} ($j = \frac{3}{2}$) level is itself degenerate. The conduction level minima or valleys are in the $\langle 111 \rangle$ directions for Ge and are located at L_1 . The conduction minima on Si are on the Δ_1 curve and occur in the $\langle 100 \rangle$ directions with k value slightly less than that of the X_1 levels. In Ge and Si, X_1 is a degenerate level.

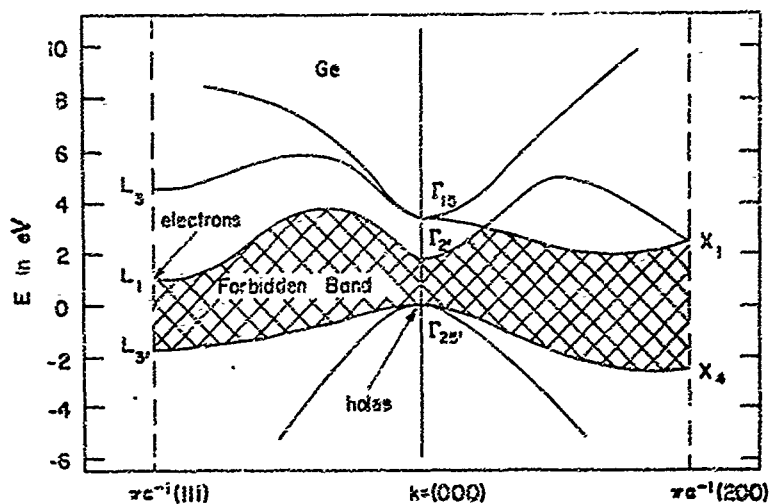


Figure 6.7: Energy Band Structure of Germanium for the $\langle 111 \rangle$ and $\langle 100 \rangle$ Directions in k-space.

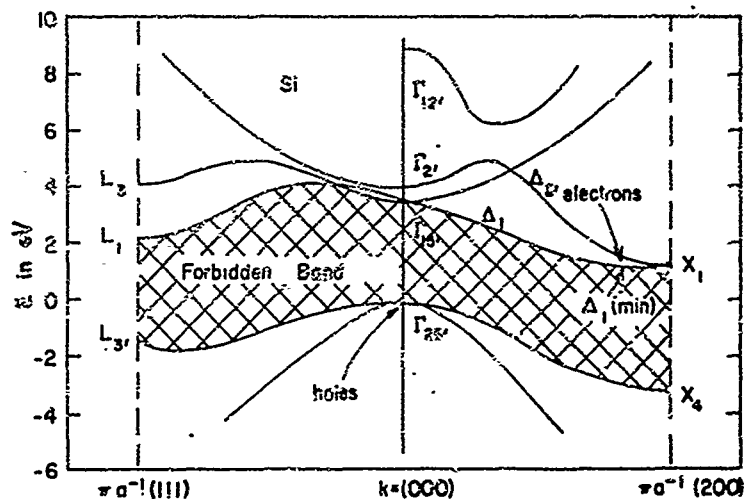


Figure 6.8: Energy Band Structure of Silicon for the $\langle 111 \rangle$ and $\langle 100 \rangle$ Directions in k-space.

As one would expect, mechanical deformation of a crystal destroys the lattice periodicity and the energy bands will change. The change is described by using deformation potential coefficients $[]$ which are defined by

$$E = E_0 + \sum_{s=1}^6 []_s e_s \quad (6.66)$$

where E is the energy at the band edge point, E_0 is the unstrained energy, and e_s are the strain components referred to crystal axes.

The allowed energy levels are found by determining the eigenvalues of the Hamiltonian. The energy change, ΔE , is defined by

$$\Delta E = E - E_0 \quad (6.67)$$

The changes in the valence and conduction band of Ge and Si are summarized below:

Valence Band of Ge and Si

$$\begin{aligned} \Delta E_{V1} = D_d e + \left(\left(\frac{2}{3} D_u \right)^2 (e_1^2 + e_2^2 + e_3^2 - e_1 e_2 - e_1 e_3 - e_2 e_3) \right. \\ \left. + \left(\frac{2}{3} D_u' \right)^2 (e_4^2 + e_5^2 + e_6^2) \right)^{\frac{1}{2}} \end{aligned} \quad (6.68)$$

$$\begin{aligned} \Delta E_{V2} = D_d e - \left(\left(\frac{2}{3} D_u \right)^2 (e_1^2 + e_2^2 + e_3^2 - e_1 e_2 - e_1 e_3 - e_2 e_3) \right. \\ \left. + \left(\frac{2}{3} D_u' \right)^2 (e_4^2 + e_5^2 + e_6^2) \right)^{\frac{1}{2}} \end{aligned} \quad (6.69)$$

where E_{V1} is the "heavy" hole band and E_{V2} is the "light" hole band.

Conduction Band of Ge

$$\Delta E_{C1} = ([]_d + \frac{1}{3} []_u) e + \frac{1}{6} []_u (e_4 + e_5 + e_6) \quad (6.70)$$

$$\Delta E_{C2} = ([]_d + \frac{1}{3} []_u) e + \frac{1}{6} []_u (e_4 - e_5 - e_6) \quad (6.71)$$

$$\Delta E_{C3} = ([\downarrow]_d + \frac{1}{3}[\uparrow]_u) e + \frac{1}{6}[\downarrow]_u (-e_4 + e_5 - e_6) , \quad (6.72)$$

$$\Delta E_{C4} = ([\downarrow]_d + \frac{1}{3}[\uparrow]_u) e + \frac{1}{6}[\downarrow]_u (-e_4 - e_5 + e_6) , \quad (6.73)$$

where E_{C1} is the conduction minimum in the $[111]$ and $[\bar{1}\bar{1}\bar{1}]$ directions, E_{C2} is the minimum in the $[1\bar{1}\bar{1}]$ and $[\bar{1}11]$ directions, E_{C3} is the minimum in the $[\bar{1}11]$ and $[111]$ directions, E_{C4} is the minimum in the $[111]$ and $[\bar{1}\bar{1}\bar{1}]$ directions.

Conduction Band of Si

$$\begin{aligned} \Delta E_{C1} = & [\downarrow]_d e + [\uparrow]_u e_1 - ([\downarrow]_u' e_4)^2 / \Delta E ; \quad |e_4| \leq \Delta E / (2[\downarrow]_u') \\ & [\downarrow]_d e + [\uparrow]_u e_1 + \frac{\Delta E}{4} - [\downarrow]_u' e_4 ; \quad |e_4| > \Delta E / (2[\downarrow]_u') \end{aligned} \quad (6.74)$$

$$\begin{aligned} \Delta E_{C2} = & [\downarrow]_d e + [\uparrow]_u e_2 - ([\downarrow]_u' e_5)^2 / \Delta E ; \quad |e_5| \leq \Delta E / (2[\downarrow]_u') \\ & [\downarrow]_d e + [\uparrow]_u e_2 + \frac{\Delta E}{4} - [\downarrow]_u' e_5 ; \quad |e_5| > \Delta E / (2[\downarrow]_u') \end{aligned} \quad (6.75)$$

$$\begin{aligned} \Delta E_{C3} = & [\downarrow]_d e + [\uparrow]_u e_3 - ([\downarrow]_u' e_6)^2 / \Delta E ; \quad |e_6| \leq \Delta E / (2[\downarrow]_u') \\ & [\downarrow]_d e + [\uparrow]_u e_3 + \frac{\Delta E}{4} - [\downarrow]_u' e_6 ; \quad |e_6| > \Delta E / (2[\downarrow]_u') \end{aligned} \quad (6.76)$$

where E_{C1} is the conduction minimum in the $[100]$ and $[\bar{1}00]$ directions, E_{C2} is the conduction minimum in the $[010]$ and $[0\bar{1}0]$ directions, E_{C3} is the minimum in the $[001]$ and $[00\bar{1}]$ directions.

Referring to the set of Eqs. 6.70-6.73 and to Eqs. 6.74-6.76 it is seen that for a general strain some of the conduction minima increase in energy while others decrease. This means that electrons will populate the lowest minima and depopulate the higher minima. Likewise the valence levels shift relative to each other as shown by Eqs. 6.68 and 6.69. Again

the holes will populate the higher energy level. The band gap E_g is defined as the difference in energy between the lowest conduction minimum and the highest valence maximum. For hydrostatic pressure all of the conduction levels shift the same amount. Likewise the valence levels shift together. The shift of E_g with strain is then simply the change in the conduction levels minus the change in the valence levels.

Table 6.7 lists the changes in the conduction and valence levels for a hydrostatic, uniaxial [100], uniaxial [111], and uniaxial {011} compression stress. As shown, the effect of uniaxial stress is considerably different from that of a hydrostatic stress. Uniaxial stresses generally cause a splitting of degenerate levels while hydrostatic stresses do not.

Using these changes of energy level and Eq. 6.57, the theoretical relation of $\gamma_v(e)$ vs stress is plotted in Fig. 3.4 for Ge and 3.5 for Si.

6.6.2 Effect of Stress on III-V Semiconductors

The III-V compounds crystallize in the zinc-blend structure which, like diamond, has face-centered cubic translational symmetry and its inverse lattice is body-centered cubic. The first Brillouin zone has the form of the truncated octahedron similar to Ge and Si. The zinc-blend structure has two different atoms per unit cell and as a result does not have inversion symmetry. This lower symmetry affects the band structure removing some of the degeneracies which occur in diamond-type crystals.

The major features of the energy band structure of III-V compounds are similar to those of Ge and Si. Neglecting spin-orbit interaction, the hole bands of III-V compounds are composed of three energy bands which can be thought of as arising from the three bonding p-orbitals (p_x , p_y , p_z) of

Table 6.7: Relative Change in the Conduction and Valence Energy Levels in 10^{-7} ev/psi as a Function of Hydrostatic and Uniaxial [100], [111], [011] Stress

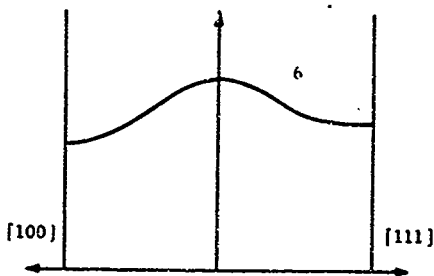
Energy Levels	Stress Orientation			
	Hydrostatic	[100]	[111]	[011]
Germanium				
$\Delta E_{V1} - \Delta E_{C1}$	-3.45	0.60	7.55	4.08
$\Delta E_{V1} - \Delta E_{C2}$	-3.45	0.60	1.29	4.13
$\Delta E_{V1} - \Delta E_{C3}$	-3.45	0.60	1.29	0.11
$\Delta E_{V1} - \Delta E_{C4}$	-3.45	0.60	1.29	0.11
$\Delta E_{V2} - \Delta E_{C1}$	-3.45	-2.95	3.36	-2.46
$\Delta E_{V2} - \Delta E_{C2}$	-3.45	-2.95	-5.47	-2.46
$\Delta E_{V2} - \Delta E_{C3}$	-3.45	-2.95	-5.47	-6.47
$\Delta E_{V2} - \Delta E_{C4}$	-3.45	-2.95	-5.47	-6.47
Silicon				
$\Delta E_{V1} - \Delta E_{C1}$	1.03	6.23	1.11	-1.33
$\Delta E_{V1} - \Delta E_{C2}$	1.03	-1.22	1.11	2.38
$\Delta E_{V1} - \Delta E_{C3}$	1.03	-1.22	1.11	2.38
$\Delta E_{V2} - \Delta E_{C1}$	1.03	4.38	-0.44	-2.96
$\Delta E_{V2} - \Delta E_{C2}$	1.03	-3.07	-0.44	0.766
$\Delta E_{V2} - \Delta E_{C3}$	1.03	-3.07	-0.44	0.766

of the atoms. These three bands are degenerate at $\vec{k} = (0, 0, 0)$ since they are simply transformed into each other by the cubic symmetry at that point. Each band is also spin-degenerate, so there is six-fold degeneracy altogether.

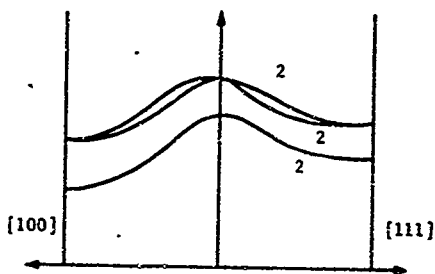
The spin-orbit interaction causes a splitting of these bands, into heavy and light hole bands and a split-off band which is slightly lower in energy than the other two bands [Refs. 62, 63]. For Ge and Si which have inversion symmetry at $\vec{k} = (0, 0, 0)$, $\nabla_{\vec{k}} E(\vec{k})$ is zero at the origin of \vec{k} space and a local minimum or maximum exists in the band structure [Ref. 58]. For III-V compounds, the inversion symmetry is missing and the energy bands are no longer required to have zero slope at the origin. The energy band structure, however, does remain symmetrical in k -space even when inversion symmetry is missing, i.e., $E(-\vec{k}) = E(\vec{k})$ [Ref. 65]. Typical hole energy band structures for the diamond structure and for the zinc-blend structure are shown in Figure 6.8. The numbers indicate the degeneracy of the various levels.

For the zinc-blend structure the non-zero slope on the energy bands at the origin of k -space implies that the maximum hole energy or the band edge points occur somewhere within the Brillouin zone. For most of the III-V compounds, however, the band edge points apparently occur very close to $\vec{k} = (0, 0, 0)$ [Ref. 65]. Figure 6.10(a) shows expanded sketches of the hole energy bands near $(0, 0, 0)$ for zinc-blend structures.

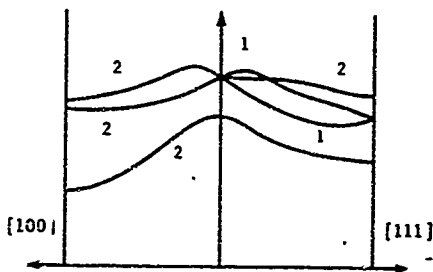
A detailed treatment of the effects of stress on the energy band structure of III-V compounds comparable to that of Ge and Si has apparently not been made prior to this contract. Because of the cubic symmetry, the effect of stress on the energy band structure at $(0, 0, 0)$



- a. Spin-orbit interaction neglected (all face-centered cubic lattices)

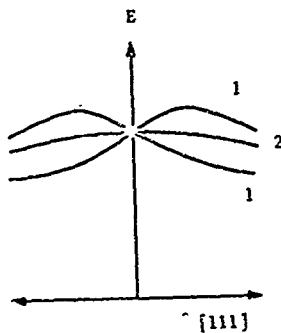
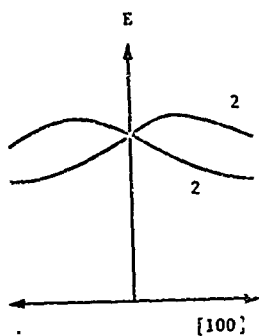


- b. Spin-orbit interaction included (diamond structure)

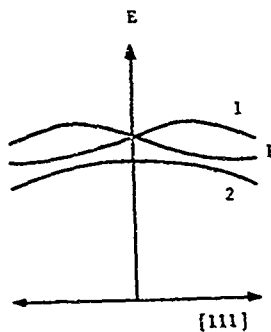
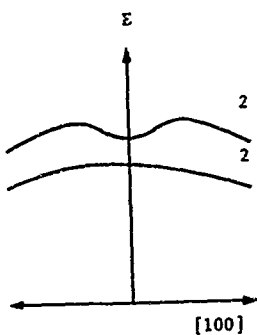


- c. Spin-orbit interaction included (zinc-blend structure; III-V compounds)

Figure 6.9: Hole Energy Band Structure



a. No stress



b. Stress in [100] or [111] directions

Figure 6.10: Hole Energy Band Structure under Stress for Values of k near $k = (0, C, 0)$. (Split-off Band is not Shown.)

is similar to that of Ge and Si, and the splitting of the energy levels with stress can be described by three deformation potentials D_d^v , D_u , and D'_u . A detailed treatment of the energy band structure without stress has been made by Dresselhaus using the $\vec{k} \cdot \vec{p}$ perturbation approach [Ref. 65]. It is possible to use this information to gain an indication of how the energy bands are split under stress for small values of \vec{k} near (0, 0, 0). The $\vec{k} \cdot \vec{p}$ perturbation matrix for cubic symmetry is similar to the strain perturbation matrix. In the $\vec{k} \cdot \vec{p}$ perturbation, second order terms in k appear in the form $k_i k_j$. The strain perturbation has similar terms of the form e_{ij} . Recognizing the similarity between the strain perturbation and the $\vec{k} \cdot \vec{p}$ perturbation, it is possible to obtain from Dresselhaus's work the following expressions for the energy bands at small values of \vec{k} and for particular stress directions:

(a) Stress in [100] direction; k in [100] direction

$$E_v = D_d^u e + \left\{ \left(\frac{2}{3} D_u \right)^2 (e_1 - e_2)^2 + C^2 k^2 \right\}^{1/2} \text{ (double roots)} \quad (6.77)$$

(b) Stress in [111] direction; k in [111] direction

$$E_v = D_d^u e + \begin{cases} (D'_u) e_4' \text{ (double root)} \\ (D'_u) e_4 + \sqrt{2} Ck \\ (D'_u) e_4 - \sqrt{2} Ck \end{cases} \quad (6.78)$$

Note that for $k = 0$, these expressions reduce to the same form as for Ge and Si. From these solutions, the shape of the energy bands under stress is sketched in Figure 6.10(b). As can be seen in the figure, the major effect of stress is a splitting of the 4 fold degenerate level at (0, 0, 0) into two doubly degenerate levels at (0, 0, 0).

For piezjunction phenomena, the important effect of stress is the shift of the band edge points and the accompanying changes in minority carriers [Ref. 25]. As long as the hole band-edge points for III-V compounds occur near (0, 0, 0), the normal equations used to describe stress effects in Ge and Si can be used as good approximations with appropriate deformation potentials.

The majority of III-V compounds (GaAs, GaSb, InP, InAs, InSb) are direct band-gap materials with the conduction band minimum occurring at (0, 0, 0). The effect of stress on the conduction band is then described by a single deformation potential, i.e., $E_C = D_d^C e$. The effect of hydrostatic stress is to change the band-gap by the amount $\Delta E_g = (D_d^C - D_d^V) e$.

Neglecting the relatively minor differences discussed above between the band structure of III-V compounds and Ge or Si, the changes in the energy between the conduction band and the two valence bands for III-V compounds are

$$\begin{aligned} \Delta(E_C - E_V) = (D_d^C - D_d^V) e \pm \left\{ \left(\frac{2}{3} D_u \right)^2 (e_1^2 + e_2^2 + e_3^2 \right. \\ \left. - e_1 e_2 - e_1 e_3 - e_2 e_3) + \frac{1}{3} (D_u')^2 (e_4^2 + e_5^2 + e_6^2) \right\}^{\frac{1}{2}} \end{aligned} \quad (6.79)$$

For the [100], [111], and [110] directions of stress, this becomes [Ref. 65]

$$\Delta(E_C - E_V) = (D_d^C - D_d^V) (s_{11} + 2s_{12})S \pm 8E \quad (6.80)$$

where S is the magnitude of stress and s_{ij} are compliance coefficients, and where

$$\Delta E = \begin{cases} \frac{2}{3} D_u (s_{11} - s_{12}) S & \text{for [100] stress} \\ \frac{1}{3} D'_u s_{44} S & \text{for [111] stress} \\ \frac{1}{2} \left[\left(\frac{2}{3} D_u \right)^2 (s_{11} - s_{12})^2 + \frac{1}{3} (D'_u)^2 s_{44}^2 \right]^{\frac{1}{2}} T & \text{for [110] stress.} \end{cases} \quad (6.81)$$

For the majority of III-V compounds, all the deformation potentials are not known so it is not possible to make detailed calculations of stress effects. GaAs is an exception in which all the necessary quantities have been determined. The deformation potentials and compliance coefficients are shown below [Refs. 66, 67]:

$$\begin{aligned} D_d^c - D_d^v &= 8.7 \text{ ev} & s_{11} &= 8.1 \times 10^{-8} (\text{psi})^{-1} \\ D_u &= 3.15 \text{ ev} & s_{12} &= -2.52 \times 10^{-8} (\text{psi})^{-1} \\ D'_u &= 5.63 \text{ ev} & s_{44} &= 11.6 \times 10^{-8} (\text{psi})^{-1} \end{aligned}$$

For compressive stress of magnitude S these give the following changes in the separation between the conduction band and the two hole bands:

(a) [100] stress

$$\Delta E_g^{1,2} = \begin{Bmatrix} 4.89 \text{ S} \\ 0.428 \text{ S} \end{Bmatrix} (10^{-7} \text{ ev/psi}) \quad (6.82)$$

(b) [111] stress

$$\Delta E_g^{1,2} = \begin{Bmatrix} 3.95 \text{ S} \\ 1.36 \text{ S} \end{Bmatrix} (10^{-7} \text{ ev/psi}) \quad (6.83)$$

(c) [110] stress

$$\Delta E_g^{1,2} = \begin{Bmatrix} 4.85 \text{ S} \\ 0.47 \text{ S} \end{Bmatrix} (10^{-7} \text{ ev/psi}) \quad (6.84)$$

For all the above stress orientations, the theory predicts an increase in the energy gap between the conduction level and both valence levels. This arises because the splitting of the valence levels under non-hydrostatic stress is not sufficient to overcome the increase in the band-gap due to the hydrostatic component of stress.

Using the above values of changes in energy gap, the ratio of stressed to unstressed minority carrier density can be calculated. This ratio, $\gamma_v(c)$, is determined by the relation

$$\gamma_v(c) = \frac{m_{V1}^{3/2}}{(m_v^*)^{3/2}} \exp\left[-\frac{\Delta(E_C - E_{V1})}{kT}\right] + \frac{m_{V2}^{3/2}}{(m_v^*)^{3/2}} \exp\left[-\frac{\Delta(E_C - E_{V2})}{kT}\right] . \quad (6.85)$$

Using the approximation

$$m_{V1}^{3/2} = m_{V2}^{3/2} = \frac{1}{2} (m_v^*)^{3/2} , \quad (6.86)$$

this can be reduced to

$$\gamma_v(c) \simeq \frac{1}{2} \left\{ \exp\left(-\frac{\Delta E_{F1}}{kT}\right) + \exp\left(-\frac{\Delta E_{F2}}{kT}\right) \right\} . \quad (6.87)$$

This equation is plotted in Figure 6.11.

The piezojunction phenomena is normally observed by stressing a small region of a p-n junction--the small area being used in order to achieve high stress levels with small forces. In Ge and Si stress causes a decrease in the band-gap and consequently very large increases in the current flow through the stressed area. The effect can be observed because the current can increase by several orders of magnitude which is sufficient to overcome the area ratio factor between the

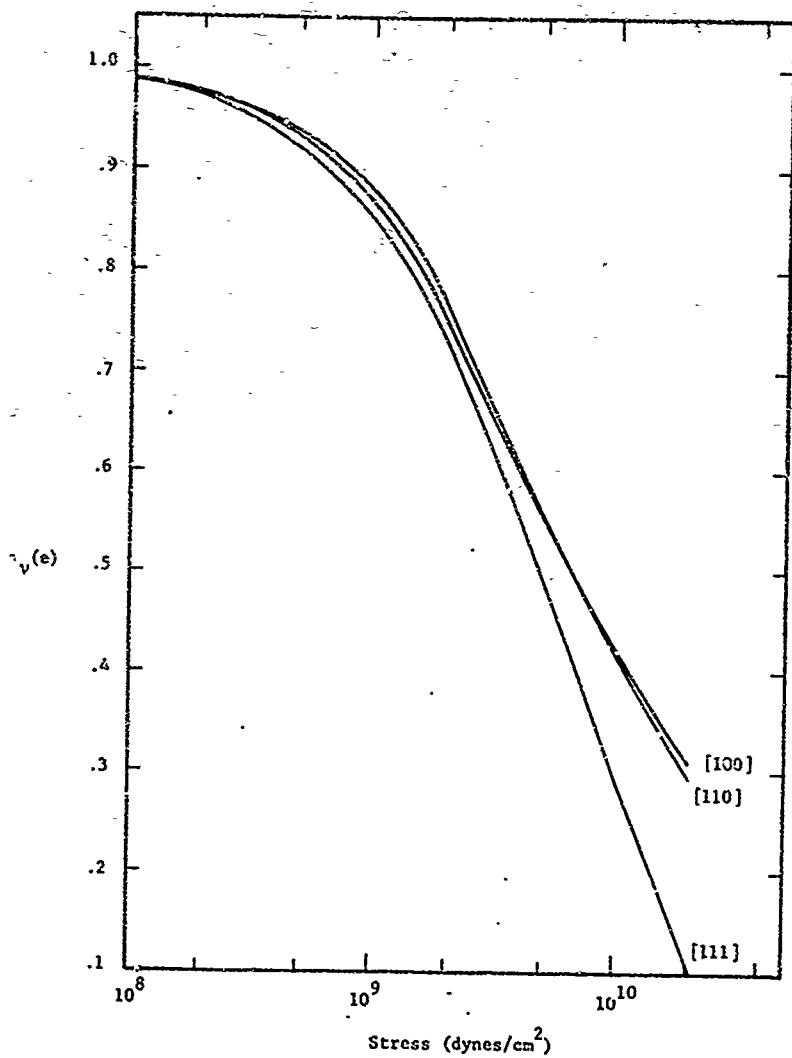


Figure 6.11: Ratio of Stressed to Unstressed Minority Carrier Density for GaAs as a Function of Uniaxial Compression.

stressed and unstressed regions. In GaAs the current in a small stressed area should decrease because of the increased band-gap, and the maximum change in current which can be observed is

$$\left. \frac{\Delta I}{I} \right|_{\max} = (A - A_s)/A, \quad (6.88)$$

where A is the total junction area and A_s is the stressed area. Thus, unless the stressed area is a significant part of the total junction area, very small current changes should be observed for GaAs devices.

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